INTERMODULATION-BORN SPURIOUS COMPONENTS IN FRACTIONAL-N FREQUENCY SYNTHESISERS

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Abstract: Spectral purity of fractional-N frequency synthesisers is affected by a set of discrete spurious components. This paper investigates the intermodulation mechanism in fractional-N frequency synthesisers and proves it is responsible for the production of these components. The number and distribution of these components are predicted by analysis of an intermodulation model and then are confirmed by numerical simulation and circuit level simulation with realistic PLL designs for the DCS application. By analysis and simulation results, potential methods to optimise the spectral purity of fractional-N frequency synthesisers are proposed.

1. Background

Fractional-N PLL frequency synthesiser is widely used in modern communication systems. Compared to integer-N frequency synthesiser, fractional-N synthesiser can achieve finer frequency resolution than the reference frequency without causing longer switching times and less suppression of VCO phase noise. A general comparison of three frequency synthesis techniques: Direct Digital Synthesis(DDS), Phase locked Loop(PLL) and Fractional-N frequency synthesis is given by Neol, *et al*[1].

In a fractional-N synthesiser, the division ratio is periodically altered between N and N+1, controlled by the overflow of an accumulator. When the overflow signal is 1, a cycle of VCO output is removed in the divider. So the instantaneous division ratio changes from N to N+1. By changing the initial accumulator input value X, the average division ratio can varies between N and N+1 as a fractional value. In this method, finer frequency resolution than integer-N synthesiser can be achieved.

From its emergence, fractional-N synthesiser is suffered from a set of discrete spurious components that degrade spectral purity. It's one of its major disadvantages. Until recently[2], it's believed that the periodical alternation of division ratio is the main source of those discrete spurious components, or fractional spurs. The alternating division ratio generates a sawtooth phase error. The sawtooth phase error gives rise to an ac output from phase/frequency detector, which modulates VCO and results fractional spurs. To remove these fractional spurs, Miller, *et al*[3] and Riley, *et at*[4] introduced ΣΔ technique into fractional-N synthesiser loop. The accumulator is replaced by a ΣΔ modulator, which converts the fractional component of division ratio into a bitstream. By the noise shaping character of

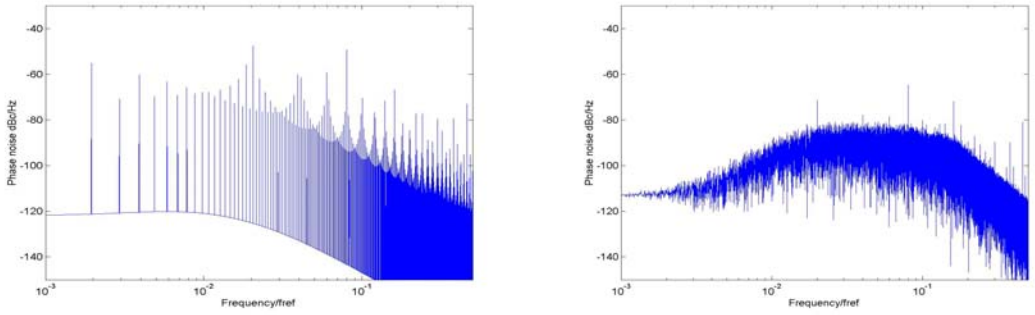


Fig.1 *VCO phase noise profile of a third order type II fractional-N synthesiser; output frequency=1809.2 MHz, reference frequency=20 MHz, loop natural frequency=250 KHz; (a) divider controlled by an accumulator; (b) divider controlled by a third order signal loop ΣΔ modulator*

ΣΔ modulator, the discrete spurious tones is converted into coloured noise[3], and is suppressed at small offsets to be rejected by loop filter. In Fig. 1 we can clearly see the improvement in spectral purity thanks to ΣΔ modulator.

From real circuit measurement we found [5], apart from the ac component generated by periodical alternation of division ratio, there is another source of fractional spurs in fractional-N loop. The detailed investigation of intermodulation-born fractional spurs was firstly published in 2003 [2]. Because there are two non-harmonically-related frequencies the reference frequency f_{ref} and the VCO output frequency f_{VCO}, existing in the loop, if these two frequencies present at a point simultaneously, intermodulation may result.

2. Intermodulation in fractional-N frequency synthesiser

A simple model of intermodulation is shown in Fig.2. In this model, the VCO output signal, with frequency $f_{VCO,}$ cross-couples to the divider output signal with frequency f_{ref} at divider output, through a cross-coupling path. It causes a series of time jitter, $\Delta t(n)$, shown in Fig.3. This series of time jitter is introduced to the phase/frequency detector(PFD), and then is converted into voltage fluctuation, imposed on loop filter. Because f_{VCO} and f_{ref} is not harmonically related, the output voltage of PFD consists of ac component, which can not be completely removed by loop filter. The ac component modulates VCO, resulting fractional spurs.

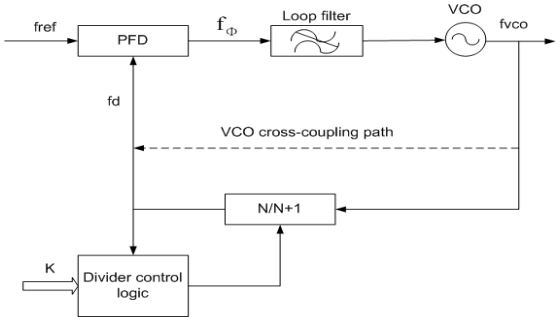


Fig.2 *Basic structure of fractional-N synthesiser with a VCO cross-coupling path*

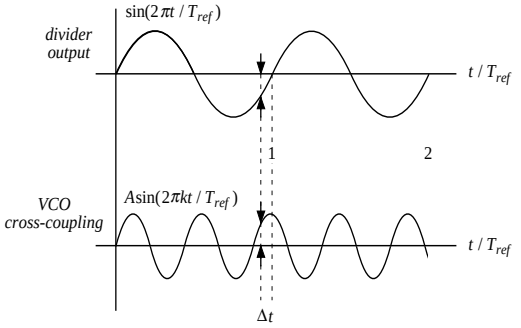


Fig.3 *Effect of VCO cross-coupling onto frequency divider output*

According to Fig.3, the divider output signal can be express as $\sin(2\pi t / T_{ref})$, where T_{ref} is the period of reference frequency; the cross-coupling signal can be express as $C\sin(2\pi kt / T_{ref})$, where C is the cross-coupling rate, k is the division ratio. k is a fractional value, consisting of integer part N and fractional part α. From Fig.3 we can easily get this equation [6]

$$\sin(2\pi\Delta t(n) / T_{ref}) + C\sin[2\pi k(n + \Delta t(n) / T_{ref})] = 0 \tag{1}$$

Writing $x_n = 2\pi\Delta t(n) / T_{ref}$, this equation becomes

$$\sin x_n = -C\sin(kx_n + 2\pi kn) \tag{2}$$

Normally the cross-coupling rate C is very small, $C \ll 1$. So x_n can be approximately expressed as a series in powers of C, given by

$$x_n = Cp_n + C^2 q_n + C^3 r_n + \ldots \tag{3}$$

Substituting (3) in (2) and using Maclaurin series for the sine and cosine functions, p_n, q_n and r_n can be worked out and then x_n can be approximated by the Fourier series

$$x_n = -C\sin(2\pi kn) + \frac{1}{2}C^2 k\sin(4\pi kn) - \frac{1}{24}C^3(9k^2 - 1)\sin(6\pi kn) \tag{4}$$

to order C^3. If $k \gg 1$, it is apparent that at each order of C the terms with the highest powers of k dominate. So equation (4) can be further simplified as

$$x_n \approx -C\sum_{m=1}^{\infty}\frac{(-mCk/2)^{m-1}}{m!}\sin(2m\pi kn) \tag{5}$$

Calculating the Fourier transform X_m of x_n, from equation (5) we can clearly see the amplitude $|X_m|$ is given by

$$|X_m| = \frac{C}{2}\frac{(mCk/2)^{m-1}}{m!} \tag{6}$$

Where the frequencies of these components are related to m by

$$\pm m\alpha + \frac{f}{f_{ref}} = \text{integer} \tag{7}$$

By scaling this result by the divider gain k and the loop filter response, we can get the effect of $\Delta t(n)$ on the VCO output, in terms of both frequency and distribution of spurious components.

3. Behaviour simulation of intermodulation

The model discussed in part 2 is simulated in Matlab. A realistic PLL design for DCS application is used for this simulation. This design includes a third order type II loop filter, and a third order single loop ΣΔ modulator as division controller. In this simulation, the reference frequency is set to 20 MHz and the VCO output frequency 1809.2 MHz. The cross-coupling rate C=0.01, or -40 dB. The result is shown in Fig.4. In Fig.4 we can clearly see the spurs generated by intermodulation, when the loop bandwidth is 100 KHz, the highest spur level is -53 dB. If the loop bandwidth is increased to 250 KHz, the highest spur level is even -37.7 dB. This seriously degrades a frequency synthesiser's performance. We also found that these spurs distribute equally with spacing of 400 KHz, or 0.02f_{ref}.

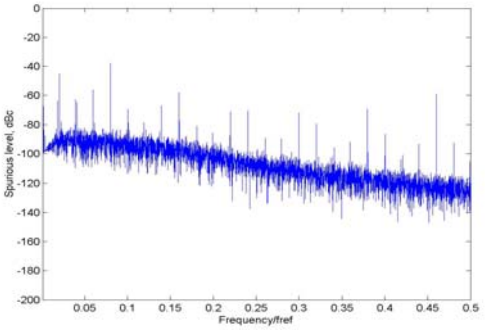
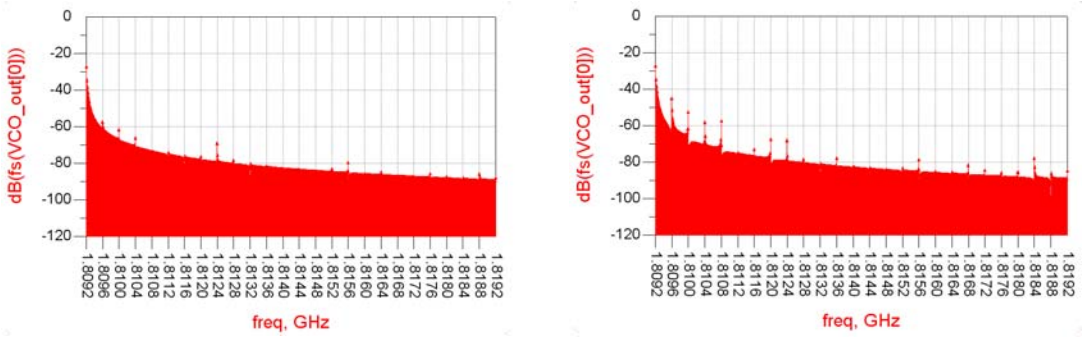


Fig.4 *VCO phase noise profile of a third order type II fractional-N synthesiser with cross-coupling between VCO output and divider output*



(a) (b)

Fig.5 *HP ADS modelled VCO phase noise profile of a third order type II fractional-N synthesiser; output frequency=1809.2 MHz, reference frequency=20 MHz, loop natural frequency=250 KHz; (a) cross-coupling rate=-100 dB; (b) cross-coupling rate=-50 dB*

A similar frequency synthesiser is modelled in HP ADS with the same reference frequency value and division ratio. The loop bandwidth is set to 250 KHz. A cross-coupling path between the VCO output and the divider output is built with a changeable cross-coupling rate. When the cross-coupling rate is set to -100 dB, in Fig.5(a) we can see the highest spur level is slightly higher than -60 dB. If the cross-coupling rate is increased to -50 dB, the spurs become significant, shown in Fig.5(b). The highest spur level increases to -43 dB. In both simulation results, the distribution of spurs is the same as the result of Matlab model. This result suggests again how a moderate amount of VCO cross-coupling degrades the performance of a fractional-N synthesiser.

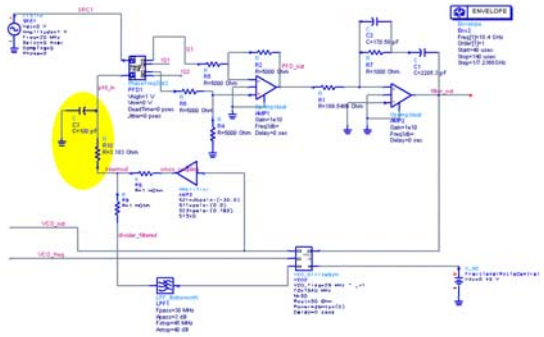


Fig.6 *HP ADS model of a third order type II fractional-N synthesiser, with cross-coupling rate at -50 dB and a passive low-pass filter at the PFD input*

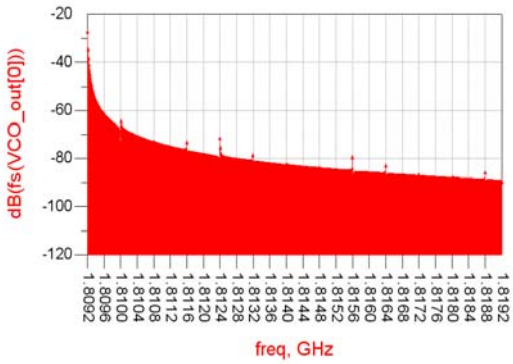


Fig.7 *HP ADS modelled VCO phase noise profile of a third order type II fractional-N synthesiser with cross-coupling rate at -50 dB and a passive low-pass filter at the PFD input*

In further HP ADS model simulation, a simple, passive low-pass filter is built at the PFD input, shown in Fig.6. The cut off frequency of this filter is 100 MHz, through which the cross-coupling VCO output signal is removed. Keep the cross-coupling rate at -50 dB and the loop bandwidth at 250 KHz, from Fig.7 we found the number of spurs is remarkably reduced, and the highest spur level is decreased to -65 dB. This result shows a potential approach in practice to reduce both the number and the level of spurious components generated by intermodulation.

4. Conclusions

From the preceding discussions we can find out the mechanism that discrete spurious components caused by intermodulation effects existing in the synthesiser degrade the spectral purity of fractional-N frequency synthesisers. A model of an potential intermodulation, based on cross-coupling between the VCO output and divider output, has been analysed and simulated to predict and prove that the number and distribution of fractional spurs depend on the fractional value of division ratio and the cross-coupling ratio. Circuit level modelling has been established and simulated in ADS. A potential method to improve spectral purity by judicious filtering is proposed. This can be supported by ADS models and realistic circuit experiments.

5. References

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