Line Simulator (LiSi) for Asymmetric and Very High-Speed Digital Subscriber Line

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Abstract: *A brief introduction describing the need for a ADSL/VDSL Line Simulator and an overview of the aim of the LiSi project followed by an overview of the history and the technology behind ADSL/VDSL is given. Also in this paper the ADSL/VDSL Line Simulator design criteria are discussed followed by a discussion of the actual circuit implementation. S/W suggestions for the creation of the three main signals needed for the ADSL/VDSL Line Simulation and finally the Testing procedure for the implemented LiSi system is discussed.*

1. Introduction.

In order to test ASDL modems in a laboratory engineers use very big twisted pair copper wire coils of several kilometers. LiSi is circuit which will simulate a twisted pair copper wire of a given length so engineers can connect it to their V/ADSL modems and test them without having to carry big coils around. This application can go even further if connected to a portable computer.

Twisted pair copper wire has certain properties, which cause problems when caring high bandwidths over long distances, these properties or effects are going to be studied in depth during the development of this project. The three main effects, that one meets when utilizing long length twisted pair copper wire for broad band data transmission, are: noise, crosstalk, and attenuation. There is also a fourth very important effect of the copper wire, which is an issue only for high frequencies thus an issue for V/ADSL, this effect is RF interference from local radio stations to the copper line.

The aim of this project is to design and construct a circuit which will simulate the effects found in long lengths of twisted pair copper wire lines for ADSL and VDSL transmission bandwidths. The Line Simulator (LiSi) is a circuit that uses as it's main component a SRAM which stores and plays-back the crosstalk, the noise, and the RF signals. The signals can be generated with the help of software written in C although this is not a requirement for this project. The three signals are added on a short line between two A/VDSL modems via a summating Op-Amp, thus the short line appears to have the properties found on a long line connection between two A/VDSL modems.

By designing LiSi, big copper coils previously used for the simulation of long-length cooper wire lines could be redundant, thus making A/VDSL modem testing easier.

2. About xDSL and background theory.

A data transmission service far speedier than anything achievable with today's dial-up modem known generally as digital subscriber line (DSL) is available. It needs only a single twisted wire-pair to provide both Internet access and conventional analogue telephony. In the very near future, it will also be used to deliver video on demand (pay-per view video) to the subscriber [1]. The most suitable version of the technology for residential broadband access to the Internet is generally held to be Asymmetric Digital Subscriber Line (ADSL).

In fact ADSL was developed for just that market. The ADSL downstream bandwidth, from the Internet to the PC at home, may reach up to 9Mbps and its upstream bandwidth, from the home PC to the Internet, may reach 640Kbps [1,2]. The asymmetry in ADSL transmission speeds matches the flow of data to and from the Internet. In a typical Internet session, on the World Wide Web the user sends short messages upstream (i.e. a mouse

click) to request data and is bombarded with information in return (i.e. video) [10]. It is this down stream transmission rate that limits the usefulness of most Internet connections.

Very High-Speed Digital Subscriber Line (VDSL) is the next and highest-Speed generation of DSL and bridges the copper telecommunications infrastructure of today with the potentially all-fiber infrastructure of the distant future. VDSL modems are placed at the end of the fiber network and in the customer's premises, respectively. When fiber terminates in a neighborhood, very high speeds are possible on the copper wiring spanning the few thousand feet from the customer to the fiber end – potentially as high as 60 Mb/s total in both directions [3,5].

2.1 Digital Subscriber Line technology.

ADSL technology was first developed in 1989 at the laboratories of Telcordia Technologies Inc., Morristown, NJ (then known as Bellcore) [1]. At that time, video-on-demand not the Internet was the prime motivator of research. In 1995, the American National standards Institute (ANSI) approved the first issue of the ADSL T1.413 standards [2]. The second issue came out in 1998. Though left dormant for some years by the phone companies the technology has recently been revived in response to the deployment of cable modems. In 1994, a trade consortium, the ADSL Forum, Fremont, Calif., was formed to promote the use of the technology.

The frequency band used for full-rate ADSL is broken into three parts: the O-4-kHz range is reserved for voice telephony, the portion between 25 kHz and 138kHz* (up to 640kHz subject to distance) for upstream data to the Internet, and the rest of the band, up to 1.1 MHz* (up to 8MHz subject to distance), for downstream data from Internet to the PCs [4,7]. (* Line distance=5.5Km on 24 AWG)

If some form of echo cancellation technology is used, the downstream bandwidth may be expanded. Echoes are signals generated by the local transmitter that get fed to the local receiver due to coupling between wires. An echo canceller takes care of echoes because it knows what was transmitted and can subtract it from what was received. But the canceller cannot help with near end cross talk (NEXT) caused by other lines in close proximity, since there is no way to know what was transmitted on those lines [4]. Beyond approximately 1 MHz*, losses in the line are so high that the frequencies are rendered unsuitable for any practical use for ADSL.

Basically, two types of ADSL modems now coexist, Carrierless Amplitude-Phase (CAP) and Discrete Multitone (DMT). They differ in how they perform line coding, that is, how they modulate digital data onto an analog carrier. CAP uses Quadrature Amplitude Modulation (QAM), in which the phase and amplitude of a pair of equal-frequency signals are varied to create between four and 1024 discrete line conditions, or symbols. Each symbol represents several bits, the actual number being dependent on the total number of possibilities [1]. For example, in a CAP- 4 scheme, with a total of four possible symbols, each symbol represents two bits. A phase of 0 degree could represent 00, 90 degrees could be 01 180 degrees would 10, and 270 degrees would be 11. In a more practical example CAP 16 uses 12 different phases and then adds a further four symbols by repeating four of the phases but at half the amplitude [6]. In this scheme, then, a total of 16 distinct combinations of patterns, starting from 0000 and ending with 1111 can be resented. Since each symbol represents four bits, CAP-16 can operate at a line speed of, say, 10 000 symbols per second (10 kilobauds) and yet transmit data at 40 kb/s.

There is, of course, a price for this efficiency. The greater the number of bits carried by each symbol, the quieter the transmission channel must be. In the case of CAP-4, with the phases 90 degrees apart, up to about 40 degrees of peak phase noise could be tolerated

without causing any errors. For CAP-12, the phase jitter would have to be below 10 degrees [1]. In CAP, only the sidebands carry any useful information. The carrier is suppressed (hence the term carrierless) and only the bands are transmitted.

With Discrete Multitone (DMT) line coding, the entire bandwidth between 0 MHz and 1.1 MHz is divided into 256 discrete subchannels, each slightly more than 4kHz wide. The first six sub-channels are reserved for analog telephony. Upstream data can occupy 24 subchannels. The downstream data takes up 248 subchannels if echo cancellation is used, and 222 if it is not.

In the middle of each subchannel is a distinct frequency (tone) kwon as a subcarrier. To transfer information, the subcarriers subject to QAM (trellis-coded modulation is an option), which can support tip to 2-15 bits per tone. The receiver adjusts itself to handle an optimal number of bits. But if noise involved, the reception of bits falls.

Whenever noise enters the system, whether as reflection from a tap (the notch in the power spectrum) or interference from a radio station, the bit per tone in those specific channels are automatically reduced using a procedure known as bit swapping. To alleviate this problem, control signals between the receiving modem and transmitting device are constantly exchanged. Note that in the presence of some kind of noise (the radio station in the power spectrum), a subchannel may even be tuned off. According to many independent experts, Discrete Multitone (DMT) is superior on several counts to Carrierless Amplitude-Phase (CAP). It is more flexible, has better noise immunity, and automatically optimizes its transmission rate with respect to line conditions in finer increments: 32-kb/s per step for DMT compared with 340-kb/s per step for CAP [8].

3. Design criteria.

3.1 Criterion (a):

The bit rate criterion is set by the DSL forum [2], and the 12Mbps data rate limit was set by Fujitsu TRC.

Copper Assess Transmission Technologies and Indicated Data Rates

Name	Meaning	Data Rate	Mode	Applications
ADSL	Asymmetric Digital Subscriber Line	1.5 to 9Mbps 16 to 640kbps	Downstream Upstream	Internet , Video on Demand, LAN, Mult/a
VDSL	Very high data rate DSL	12 to 52Mbps 1.5 to 2.3Mbps	Downstream Upstream	Same as ADSL.

Table.1: The DSL forum definitions for ADSL and VDSL.

3.2 Criterion (b):

The maximum frequency component is fmax = 12MHz.

And according to the Nyquist sampling theorem: fsample= 2*fmax.

Hence fsample= 24MHz.

This figure sets the maximum clock frequency of system oscillator at 24MHz and the maximum clocking speeds for the SRAM IC's and the DAC IC at 24MHz.

3.3 Criterion (c):

The system resolution of 16 bit was set by Fujitsu TRC, this defines the bit resolution of the two major parts of the Line Simulator: 2x8-bit SRAM, 1x16-bit DAC.

3.4 Criterion (d):

The SRAM ICs total capacity figure is 32Mb, this was set by Fujitsu TRC to be at least 16Mb. But it is also derived thus: The SRAM should have large capacity, enough to store and play back the 12MHz signal for at least 1 second in order for the random noise signal

thus the simulation to be as realistic as possible. According to calculations the 32Mb SRAM can playback signals with bandwidth 0-12MHz for 2.4 seconds.

4. System implementation.

To describe the system operation two assumptions are made:

First, only one signal parameter is considered: Random noise signal with bandwidth 0-12MHz (A/VDSL data rate). The second assumption is that the simulator is unidirectional so one direction of the modems transmission is considered, as this is a prototype circuit the same work can be done twice in order to create a bi-directional system.

4.1 Read cycle.

The A/VDSL date rate noise signal created in the S/W (see section 5) enters the Line Simulator (LiSi) via the PC parallel port. The port resolution is 8-bit wide, thus in accordance with criterion (c) the signal is multiplexed into 16 bits as it enters the first stage of LiSi. This is achieved with the use of 16 3-state buffers (4xICs: 74LS125), the signal is and the buffers are clocked with the parallel port STROBE O/P. Now the 16-bit signal enters the two 16Mb SRAM (2xICs: EDI82046C) in which is stored. The total SRAM capacity is 32Mbits set by criterion (d), both SRAM are clocked by a 21 address generator. The address generator comprises of two 12-stage counters (12+9 addresses used form two ICs: 74VHC4040). The counters are clocked by the parallel port strobe O/P for the duration of the read cycle, note that before recording the counters are reset via a 5volt pulse provided by a push button to insure the smooth operation of the recording procedure.

4.2 Write cycle.

The stored signal(s) in the SRAM are outputted via the I/O pins D0 to D15. At the same time the 3-state buffers O/Ps go to high incidence so they will not be damaged by the signals coming form the SRAM making there way to the 16-bit DAC I/Ps. The DAC (AD768) maximum sampling rate is 30Mb/s and is clocked by a 24MHz crystal clock oscillator, which also clock the SRAM ICs via the address generator for the duration of the writing cycle. The converted analog signal will now be added to a line of a few cm between two A/VDSL modems. This is done with a summing Op-Amp (AD845) which is band limited to 12.5MHz thus no separate filtering stage fore the 24MHz analog signal is needed. Finally the to connect the two modems to the summating Op-Amp, a differential to single end line receiver and a single end to differential line driver are used.

5. Software suggestions.

Creating the software for LiSi is not one of the project's requirement, as the complexity of the circuit was immense. However a few suggestions can be made at this point. One: The software can be written in C. Two: The random noise the xtalk and RF interference signal must be generated in the S/W. The noise should be of random nature and near Gaussian distributed. A for loop could be used for the reproduction of each signal Noise, RF interference and Xtalk. The exact figures for these signals can be obtained from the ETSI standards on ADSL and xDSL, Document: ETSI STC TM6, Title: "Performance tests for SDSL, ADSL and other long-range xDSL systems.

6. Testing procedure.

This system will be implemented on a PCB when this is ready the test can begin.

If a signal with bandwidth 0-12MHz is stored in the SRAM and then outputted form it, this is enough to prove that the simulator works.

Procedure: First a signal of 12MHz is connected to pin D8, MSB and a signal of 500ns or 2MHz [9] in the strobe pin, form a signal generator. The Line driver O/P will be connected to an oscilloscope. If the I/P signal is present at the line driver O/P when the system is in the write mode then it can be assumed that the simulator is working so far. For the system to be proven 100% operational a second 12MHz signal, but with different amplitude and phase this time, will be feed into the I/P of the line receiver. If the O/P signal at the line driver contains both signals then that proves that the summating Op-Amp works thus all of the analog circuitry so at that stage I would be safe to assume that the system is working. The tests will continue by reducing the frequency of the input signals thus exploring the limitations of the system.

7. Summary.

This research has proven very difficult in terms of finding the discrete components to design the line simulator and this is mainly due to the technological restrains, there are not many IC manufacturers that build devices for such extreme data dates such as VDSL and ADSL.

DSL after other stages finally involved into ADSL and VDSL (not standardised yet).

ADSL is used for residential broad band Internet access and pay-per-view video services (Down and Up-stream interaction) also provides normal phone service through a twisted pair copper wire.

LiSi is a circuit, which simulates the effects found on long distance telephone copper lines when subjected to V/ADSL date rates. The purpose of this system is to make V/ADSL modems testing easier.

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References.

[1] A. D. Roy "A second wind for wiring" IEEE Spectrum, September 1999. [2] "General Introduction to Copper Access Technologies", The ADSL Forum, 1998, www.adsl_forum.com. [3] J. M. Cioffi, S. Olcer, A. Pach "Very High-Speed Digital Subscriber Line", IEEE Communications Magazine, May 2000. [4] R. F. M. van den Brink "Performance tests for SDSL, ADSL and other long-range xDSL systems", ETSI STC TM6(98)10, ETSI Standards, revision 3 November 26 1999. [5] "VDSL Tutorial, Fiber – Copper Access to the Information Highway (Early Draft)" The ADSL Forum, 1999, www.adsl_forum.com. [6] D. J. Rauschmayer, "ADSL/VDSL Principles", Macmillan, 1999. [7] "ADSL Tutorial, Twisted Pair Access to the Information Highway", The ADSL Forum,1998, www.adsl_forum.com. [8] "CAP Vs DMT ", Aware Ltd, white paper, March 1999. [9] HT6535 SPP/EPP/ECP Controller Data sheet, Holtek, p12, 25 June 1997. [10] Prof. J. O'Reilly "Introduction to Telecommunications Networks" UCL lecture module. 1999