Low Cost Open Architecture Radar Systems

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Abstract: This paper describes the design and build of a low-cost (sub £1,000) radar system for short-range surveillance applications. Specifically the viability of using Commercial Off-The-Shelf (COTS) components is considered together with interface requirements in terms of implementing "open architecture" designs. The performance of these currently available components is assessed individually and in terms of the built prototype system. The work has demonstrated the viability of this approach.

1 Introduction.

This project examines the feasibility of using current generation Commercial Off-the-Shelf (COTS) components to design a very low cost (sub £1,000) radar system for short-range general surveillance. Such a design could have many commercial applications, including marine radar, airport surface surveillance, perimeter security and roadway monitoring. In addition the issues involved in implementing true "open architecture" systems are examined, together with the potential for COTS systems to compete with higher-end military radar.

Research into low-cost modular military systems has escalated since the US Department of Defence review in the early 1990s concluded that best value could be obtained by purchasing COTS components wherever practicable in order to reduce costs and time-to-deployment [1]. The use of proprietary components with short shelf lives can make upgrades uneconomical, despite the large cost involved in developing new systems. The term "open architecture" refers to components conforming to formal interface specifications, which are fully defined by group consensus in industry and freely available to the public and manufacturers [2]. Developing radar systems based on such a model would allow compatible third-party functional replacements and upgrades to be fitted at comparatively low cost.

The project workplan was divided into two sections: firstly analysis of the suitability of currently available COTS products and their conformity to open architecture interfaces, secondly a design and build of a prototype system, plus evaluation of its performance and areas of potential improvement.

2. Radar Specification.

2.1 Radar parameters

The standard radar equation (1) establishes the relationship between range and transmission power for given parameters.

$$R_{\max} = \left(\frac{P_t G_t G_r \sigma \lambda^2 L_s}{(4\pi)^3 N(SNR)} \right)^{1/4} \qquad (1)$$

In order to establish the approximate transmission power (P_t) requirements for the prototype design, some assumptions must be made regarding the characteristics of a system suitable for the applications previously mentioned:

Maximum range ($R_{\max}$) = 200m (suitable starting point for civilian surveillance)
Antenna gain (G_t, G_r) = 300 (typical for ideal 1m^2 area dish at nominal 1.5GHz RF)
Radar cross section (σ) = 1m^2 (for a person or small vehicle)
RF wavelength (λ) = 0.2m (for nominal 1.5GHz RF)
Total loss (L_s) = -5dB (typical plumbing loss, filters, etc)
Mean noise power (N) = 2 * 10^{-13}W (for 50MHz band-limited thermal noise, ideal receiver)
Signal-to-noise ratio (SNR) = 13dB (nominal figure for reliable target detection).

Based on these assumptions the required mean transmission power is 120mW. The peak transmission power for a pulsed radar system is dependent on the duty cycle, i.e. pulse width (τ) * pulse repetition frequency (PRF). The PRF must be less than 750kHz for the desired unambiguous range. A very low PRF reduces the data processing requirements, but the resulting low duty cycle requires a high *peak* transmission power from the

amplifier, and doppler processing may necessitate a higher rate - values of 1 to 10kHz are common for general surveillance. A typical pulse width of 5*ms* provides range resolution of 750m, which can be improved considerably using pulse compression techniques.

2.2. System overview

Figure 1 shows a block diagram of a generic radar system with a single element using separate (but closely spaced) antennae for transmission and reception.

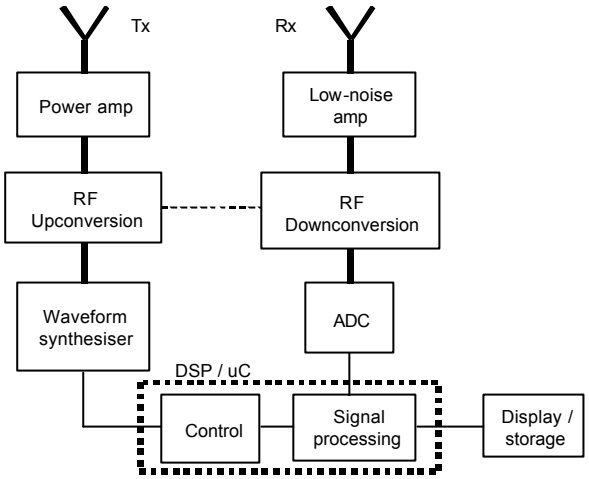

Figure 1: Generic radar system

Each block is considered a modular component, formed from one or more COTS components, preferably interfaced using open architecture methodology.

2.3 Waveform synthesiser

Radar systems transmit pulsed or continuous waveforms, modulated onto a RF carrier. The waveform is usually coded in frequency or phase (*pulse compression*) in order to achieve the dual attributes of good range resolution (implying small 'effective' pulse width) and long range (implying high mean transmitted power, or large 'actual' pulse width). The frequency synthesiser used to generate these waveforms must provide a wide output bandwidth and high *frequency agility* (switching speed between output frequencies). In addition the specification of the synthesiser must be considered in terms of noise (phase and amplitude), spur levels (spurious signals) and long-term stability.

Traditionally radar systems have used techniques based on analogue "*direct*" frequency synthesis - the output frequency produced from a bank of reference oscillators by mixing, multiplication and division [3]. However such systems are bulky and expensive in terms of hardware requirements, and the electrical switching can produce high levels of spurious signals. Alternative "*indirect*" frequency synthesisers typically use an analogue or digital phase-locked loop (PLL) with a comb generator reference oscillator. Frequency switching is achieved by applying a voltage to the tuning input of the VCO. Such synthesisers are relatively inexpensive and compact, although they suffer from slow frequency acquisition time that limits the effective bandwidth.

Direct Digital Synthesis (DDS) requires no reference oscillators - just a stable, low-jitter clock. A sine look-up table is used with a phase accumulator to provide a digital signal. An integrated digital to analogue converter (DAC) and reconstruction filter synthesise the waveform output. DDS chips are digitally programmed by writing tuning words to internal registers. The *frequency switching speed*, defined as the latency between programming a new frequency and the output settling at that new frequency [4], is very low, often as low as one clock cycle (5ns at 200MHz clock rate, which is some 1000x faster than even the latest sigma-delta digital PLL designs). However the *update rate*, defined as the rate at which the programmed frequency can be changed, is dependent on the programming method and controller.

Whilst current DDS chips do not produce the same performance levels as some custom designs, they are widely available from several manufacturers at a unit cost less than $30, and so are fast becoming the preferred synthesis method for low cost COTS systems.

2.4 RF Upconversion

Radar systems normally use a multi-stage IF approach when upconverting the modulated baseband signal to the required RF frequency using several mixer/filter stages.

An alternative to this approach, the "phasing method", is possible due to many DDS devices providing both in-phase and quadrature outputs using dual synchronous DACs. Then it is possible to directly upconvert to a single-sideband signal at relatively high IF using a quadrature modulator, thus removing the problems of unwanted image rejection. Such devices are packaged on small integrated circuits and are available from several manufacturers at unit cost of approximately $5. The IF input must be provided by a phase coherent local oscillator. Further upconversion stages can be integrated using the traditional mix/filter method where the double sideband images are more widely spaced.

2.5 Data Capture

The latest generation of general-purpose digital signal processing (DSP) chips afford the capability to perform real time signal processing and digital beamforming. Each complex sample (in-phase and quadrature) from the analogue to digital converter is equivalent to one range bin. The quadrature channel can be created in the analogue domain using a 90-degree phase shifter, in which case dual ADCs must be used, or created digitally using Hilbert transform in the DSP, in which case a single ADC can be used, albeit at twice the sampling rate for Nyquist compliancy.

Digital beamforming becomes highly attractive in phased array designs where alternative analogue methods are expensive and bulky. Digital methods allow each array element to be digitised separately [5] - data is centrally processed allowing independent beams to be formed simultaneously, high agility is possible as well as techniques for effective jamming suppression.

3. Prototype Design and Build.

Having evaluated candidate COTS products, a design for the prototype system was formulated based on the specification outlined above, in addition to the compliance of components in terms of the COTS and open architecture methodology. Figure 2 outlines the system design, including unit cost per component, interfaces and data flows.

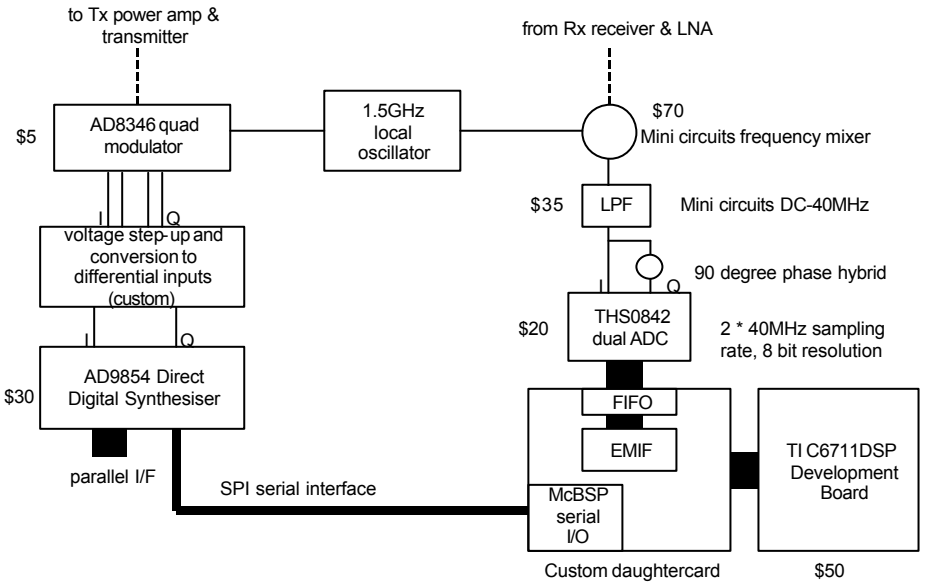

Figure 2: COTS radar design showi ng component cost and data flows

The AD9854 DDS has a maximum output bandwidth of 150MHz, although in the prototype it is constrained to 40MHz. Its registers can be programmed via Motorola SPI compatible serial interface or a higher-speed

proprietary parallel interface. This method requires considerable glue logic to interface to the DSP and does not fit well into the "open architecture" methodology, so the SPI interface was used despite its inferior performance.

The Texas Instruments C6711 DSP is the central controlling unit for the system. Specifically it programs the registers of the DDS, arbitrates data transfer from the ADC, and performs real-time digital signal processing. The C6711 development board provides headers for mounting custom daughter cards. A PCB was designed that allowed access to the SPI compatible serial I/O for the DDS, plus access to the proprietary External Memory Interface (EMIF) via a FIFO. The FIFO buffers data from the ADCs, bus matches to make best use of the 32-bit interface, and allows synchronous free-running clocks and control signals to determine when data is written to and read from the device. The C6711 controls timing of writes from the converters, performing bulk multiword DMA transfers from FIFO to SDRAM with accurate timestamps to reduce the load on the DSP.

The hardware was constructed using custom headers and ribbon cables to connect digital interfaces, and SMA coaxial connections between RF components, ready for testing in an anechoic chamber.

4. Testing and Evaluation.

The test procedure will first analyse the amplitude and phase mismatch between DDS output channels across the frequency range using an oscilloscope. This performance directly affects suppression of the carrier and unwanted image in the quadrature modulator. The resulting IF output will be measured by spectral analysis, which will also give a measure of the output phase noise (ratio of noise power to carrier power in each unit bandwidth). For the receiver, a noise generator is utilised to calculate the noise figure of the RF components, giving a measure of the reduction in SNR due to self-noise in addition to the expected thermal noise power.

The DDS will be tested to calculate the fastest speed at which changes in frequency and phase can be reliably programmed via the SPI interface, which determines the frequency agility of the system. The C6711 DSP runs multithreaded and must use interrupts to perform its processing and control/timing tasks simultaneously. Inevitably there is ISR latency when switching threads (saving stacks, loading new program pointer, etc). The real-time capability will be determined by adding processing stages and testing for a range of PRFs.

The overall performance of the system is now being evaluated against the criteria defined for likely applications - i.e. waveform agility, achievable SNR in terms of phase noise and receiver noise figure, and real-time processing (which as a function of the input data rate will determine the maximum PRF).

5. Summary.

A prototype short-range surveillance radar system has been designed and built primarily using an open architecture approach and low-cost COTS components. Initial testing is underway and suggests that many of the criteria required for a range of radar applications can be met in this way. Interfaces between components are often proprietary and some additional engineering is required in order to adopt a true "open architecture" platform. However opportunities are available to quickly design glue logic and controllers to allow these devices to be used in an open system, still at relatively low cost.

Further work will include developing an open architecture high-speed controller interface for the DDS to increase frequency agility, increasing real-time DSP performance using an FPGA solution [6] in conjunction with traditional DSP, adding electronically stepped local oscillators, and analysis of optimisations of IF/RF performance in the current design. The system will be field-tested in selected applications, and further upconversion stages will be added to allow operation at higher frequencies.

References.

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