

Effects of the Error State on Sequential Synchronizers

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Abstract: In this paper we study the effects of the error state in the jitter behaviour of the sequential synchronizer. We define the correct state as the one where the system arrives due to signal transitions and we define error state as the one where the system arrives caused by noise spikes. We will see that, when the sequential synchronizer is in the error state processes the input signal corrupted by noise with an aggravation of jitter.

1 Introduction.

In this work we will see as the sequential synchronizer can enter in the error state driving to a strong increment of the jitter [1, 2].

In the analog, hybrid and combinational synchronizers which have signal comparator without memory, the output jitter (UI) is mainly function of the input signal to noise ratio (SNR), however in the sequential synchronizer which has signal comparator with memory, the output jitter (UI) is simultaneously function of the input signal to noise ratio (SNR) and also of the signal comparator state Q (correct or error). To illustrate as the output jitter UI is function of the input SNR and of the circuit state Q, we consider the diagram of Fig.1.

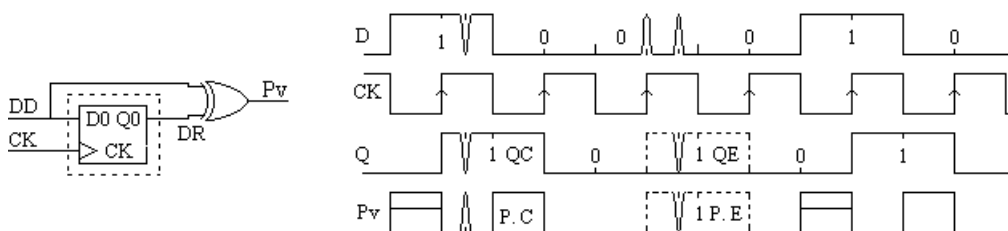


Fig.1 Impact of the error state in the jitter

The output P_v is function of the input D (signal corrupted by noise) but also of the flip flop state Q which can be correct QC or error QE .

We observe that the input signal with noise is normally processed in the correct state QC and only during T is processed in the error state QE . So normally P_v depends on the input D and on the correct state QC , but during the error pulse time PE the output P_v depends on the D input SNR and on the error state QE . This error pulse is an extra contribution to a great increment of the jitter.

The synchronizer that we go present uses the flip flop D with XOR as phase comparator to produce the variable pulse P_v and a delay circuit with XOR as monostable to produce the fixed pulse P_f . This pulse P_f annuls the DC component of the pulse P_v .

The correct pulse PC due to the signal transitions is previsible then can be generated simultaneously a reference pulse that annuls the effect DC. However the error pulse PE due to noise spikes is unexpected, then we can't generate a reference pulse to annuls the DC component what perturbs the VCO increasing its jitter.

2. Sequential symbol synchronizers.

2.1. Sequential synchronizer of both transitions

We consider the sequential symbol synchronizer of both transitions which is based on the comparison of a variable pulse P_v produced by the phase comparator against a fixed pulse P_f produced by a monostable (Fig.2) [3].

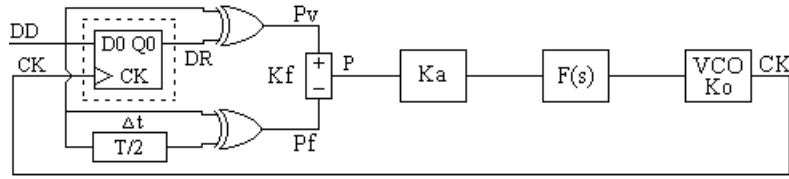


Fig.2 Sequential symbol synchronizer of both transitions

At the equilibrium point, the variable pulse P_v has the same area of the fixed one P_f , so the DC component is zero and the VCO oscillates in its free-running frequency f_0 .

When the clock frequency diminishes and the clock delays, the variable pulse P_v becomes greater than the fixed pulse P_f then the error signal P is positive what increases the VCO frequency, advancing it until P_v equates P_f . On the other hand if the clock frequency increases and the clock advances, the variable pulse area P_v becomes minor than the fixed pulse P_f then the error signal P is negative what decreases the VCO frequency, delaying it until P_v equals P_f . Fig.3 illustrates as a noise spike produces a error pulse which can be single (P.E.S.) when the sequence is favourable or duple (P.E.D.) when the sequence is unfavourable.

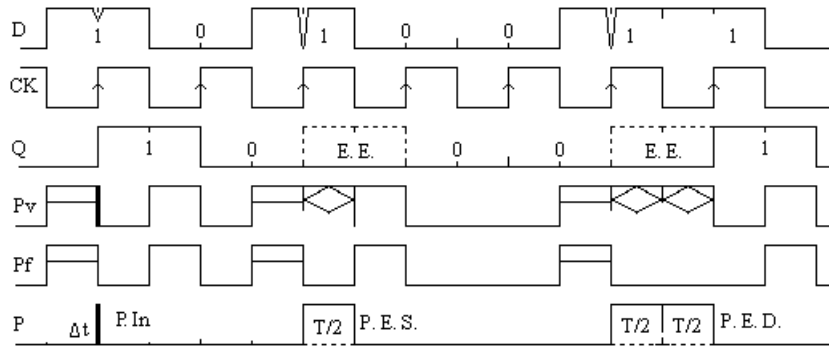


Fig.3 Waveforms at the sequential symbol synchronizer of both transitions

In the first situation (last figure left), the noise spike is ignored due to the noise margin of the gates, however can create a little perturbation P . In.

In the second situation (centre), the noise spike drives to the error state whose effect finish in the next data transition (favourable sequence 101 ...), then produces a single error pulse P.E.S. of value $T/2$.

In the third situation (right), the noise spike drives also to the error state, but its effect now only finishes in the next clock positive transition (unfavourable sequence 110011 ...), then produces a duple error pulse P.E.D of value $2 \cdot T/2$ which aggravates the jitter.

From this analysis we observe that for low SNR, the noise spikes drives to the error state provoking a jitter increment. However for high SNR the low noise spikes are ignored by the gates noise margin.

2.2. Sequential synchronizer of positive transitions

We go still to present the sequential symbol synchronizer of positive transitions, which it is based in the same principle of the one based on both transitions (Fig.4).

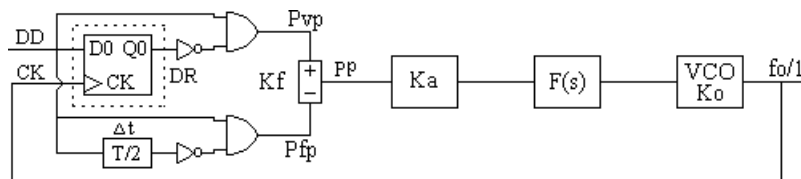


Fig.4 Sequential symbol synchronizer of positive transitions

Here the variable pulse P_v and the fixed one P_f are compared only when a data positive transition occurs. This circuit is helpful to better understand the effects of the error state in the sequential

$$Ka \frac{KfKo}{4} = Ka \frac{(1/4p)2p}{4} = 0.02\text{Hz} \rightarrow Ka = 0.08*2 \quad (4)$$

The 2nd order loop is also used in many applications

3.4. Results

Fig.9 show the clock output jitter UI (RMS Unit Intervals) as function of the input SNR (signal to noise ratio). We tested the sequential synchronizer of both transitions (tx) and the synchronizer of positive transitions (txp) with the sequence one “1” one “0” alternated (1U1Z) and with the sequence two “1” two “0” alternated (2U2Z).

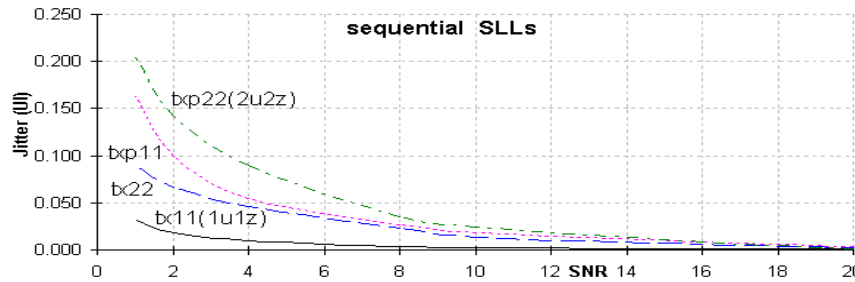


Fig.9 Jitter-noise curves of the two synchronizers (tx, txp) tested with two sequences (1U1Z, 2U2Z)

We verified that for the synchronizer of both transitions, the jitter-noise curves are good for the favourable sequence 1U1Z, but there is an aggravation with the unfavourable sequence 2U2Z.

For the synchronizer of positive transitions the sequences (1U1Z, 2U2Z) are unfavourable and then the jitter noise curves are bad.

4. Conclusions.

The sequential synchronizers, particularly the ones based in pulses comparison (triggered by VCO), posses jitter-noise curves which depends on the input sequence type.

We know that the error signal perturbations are applied to the input of the VCO originating jitter in its output. We noticed those perturbations are provoked by the input noise which manifest directly or indirectly driving to the error state, generating single error pulses P.E.S. and duple error pulses P.E.D.

The favourable sequences (101 ...) generates predominantly single error pulses and the unfavourable sequences (110011 ... or pseudo-random) generates predominantly duple error pulses that aggravates the jitter.

In the positive transition synchronizer the number of transitions considered are only half of the case of the both transitions synchronizer. So the both transitions synchronizer has a jitter performance better than the positive transitions synchronizer.

When the number of the signal transitions diminishes, decreases the probability of the single error pulses and increases the probability of the duple error pulses, which aggravates the jitter.

Acknowledgments.

The authors are thankful to the program FCT (Fundação para a Ciência e Tecnologia) for financial support.

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