Emulation of Multiple EDGE Physical Layers Using a Reconfigurable Radio Platform

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Abstract: A novel architecture for the testing of enhanced data rates for GSM evolution (EDGE) networks is proposed, in which a reconfigurable radio platform is used to implement up to 16 EDGE physical layers in a RF baseband module (RFBBM). When the RFBBM is used in conjunction with a line server unit (LSU), a complete mobile station emulator (MSE) is formed. In this paper, the implementation and interfacing of the constituent parts in the reconfigurable RFBBM are described.

1. Introduction

The Global System for Mobiles (GSM) radio interface, although originally designed to operate in the circuit-switched mode, has evolved to support high data rate packet communications. Addition of enhanced data rates for GSM evolution (EDGE) technology facilitates operation in both packet- and circuit-switched modes, with high data rates being achieved through the introduction of new modulation and coding schemes in the physical layer, and utilising link adaptation in the data layer.

Performance characterisation of equipment and networks employing EDGE technology can be achieved with the aid of a mobile station emulator (MSE), which implements conventional and extended mobile station (MS) functionality. The extended capabilities of the MSE are used to test the network concerned. MSEs commonly divide the various RF and baseband processing tasks between two modules. The first, the so-called line server unit (LSU), provides the required hardware interface to the telecommunications network whilst implementing the GSM/EDGE protocol stacks. The LSU communicates with the RF and baseband module (RFBBM) over an open interface. The RFBBM, whilst exchanging packets with the LSU, executes the physical layer baseband functions such as modulation, demodulation and synchronisation, together with RF transmission and reception. The relationship between the LSU, RFBBM and the base station being tested by the MSE is shown in Figure 1.

In this paper, we propose a novel MSE architecture in which a RF module operating at GSM frequencies and an Advanced Signal Processing Engine (ASPE) designed by Multiple Access Communications Ltd are combined to form a reconfigurable RFBBM. Implementing the RFBBM in this manner is highly advantageous, because it allows the design to be easily modified. For example, the MSE might initially be required to employ a direct cable link to the base station (BS) under test and, since the signal-to-noise ratio (SNR) will be high, there will be no need for channel decoding or equalisation. However, the addition of these functions for other test scenarios requires only a software reconfiguration via a PC card interface to the ASPE. The relationship of the ASPE to the ancillary RFBBM components, and to the LSU described above, is shown in Figure 1.

Now that the MSE architecture has been defined, we proceed to investigate in more detail the interaction between, and requirements of, the three parts of the RFBBM.

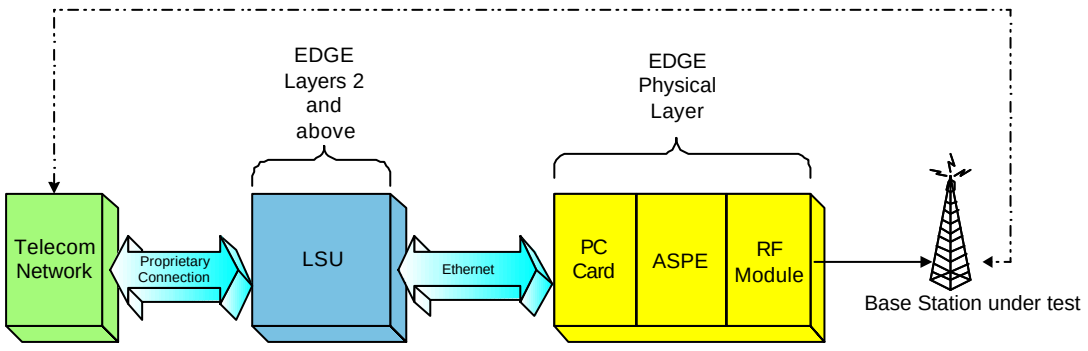

Figure 1 The basic structure of a novel MSE architecture in which the physical layer is implemented using the ASPE, a reconfigurable radio platform.

2. RFBBM Modules

2.1 Division of Processing

The reconfigurable nature of the RFBBM requires careful division of processing tasks to achieve optimum performance from each module. A task is assigned to a module on the basis of the required frequency of computation, with computations performed at the symbol rate being the most intensive. Figure 2 shows the division of processing tasks between the ASPE, RF module and PC card, together with the appropriate interface buses and ancillary components.

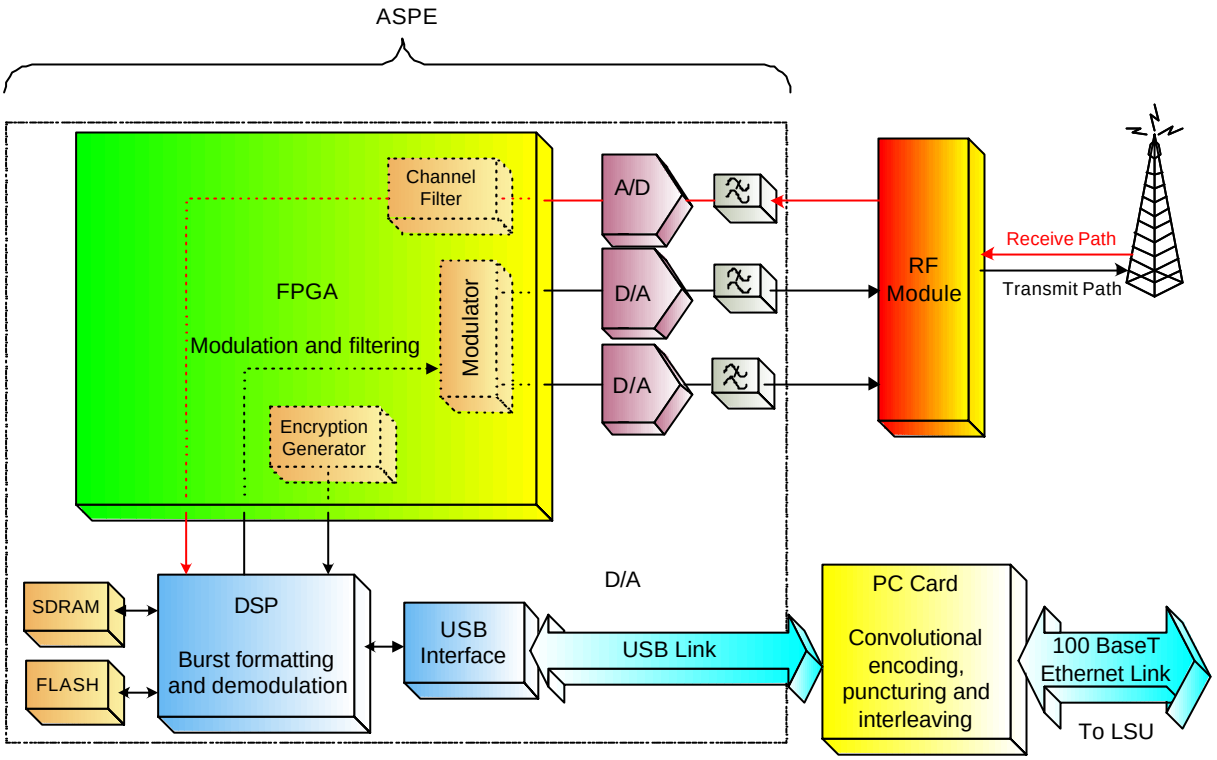

Figure 2 The division of processing amongst the constituent modules of the RFBBM, together with the appropriate interface buses and ancillary components.

Consider the transmit path of the MSE, shown in black in Figure 2. For each emulated MS an independent set of transmit processes must be implemented. These processes, as exemplified in TS05.01 [1], include channel coding, encryption, burst formatting and modulation. Channel coding, which includes puncturing and interleaving, is a bit-manipulation process that can be efficiently realised through large look-up tables. Hence the PC card, which will have memory in abundance, is ideally suited to implementing the channel coding function. Conversely, the process of encryption requires access to the current frame number, and it seems prudent to assign this task to the field programmable gate array (FPGA), as this is where the hardware frame counters reside. However, since the subsequent burst formatting is appropriately handled by the Digital Signal Processor (DSP), the encryption process is split between the FPGA and the DSP. The FPGA includes an encryption sequence generator, the output of which is read by the DSP and used to mask the data sequence prior to burst formatting. Finally, symbol rate computations, such as the pulse shaping and modulation processes, are well matched to a FPGA implementation.

On the receive path, a similar division of processing is employed. Channel filtering, a numerically intensive task, is assigned to the FPGA, whereas the less severe computational requirements of demodulation allows this function to be assigned to the DSP.

2.2 The PC Card

A PC card is a convenient hardware platform to support the ASPE. Since it includes Ethernet and universal serial bus (USB) links for communication with the LSU and the ASPE, it provides

significant processing power to enable the computational burden to be shared with the ASPE, and is well supported with development tools.

The PC card implements channel coding schemes CS1-CS4 and MCS1-MCS9 as given by TS05.03 [2]. Data and control information for each MS to be emulated will be received from the LSU via the Ethernet link. The appropriate channel coding will be performed and the resulting data buffered in readiness for transfer to the ASPE in time for transmission in the appropriate frame and slot. Since the physical layer has hard real-time constraints, it is important that the PC card and the ASPE are synchronised, however due to variable latency on the USB link some buffering of data within the ASPE will be necessary. To avoid the need for hardware synchronisation signals, a message-based synchronisation system is used in addition to the USB link. Since downlink data sent from the ASPE to the PC will be at frame rate, the reception of messages by the PC card can be used to trigger data transfer in the uplink direction. Message packets received from the ASPE will be de-interleaved and decoded before being passed on to the LSU via the Ethernet link.

Finally, the PC card will also be required to perform logging of the packets exchanged with the LSU. This is particularly important for the link adaptation process, which is initiated by the data layer but requires measurements performed by the physical layer.

2.3 The ASPE

The ASPE, as shown in Figure 2, consists of a one million gate FPGA, a 400 million instructions per second (MIPS) DSP, a USB interface to provide high-speed connectivity, a 14-bit, 80 MSample/s analogue-to-digital converter (ADC) and two 14-bit, 32 MSample/s digital-to-analogue converters (DACs) to give quadrature baseband outputs. As described in Section 2.1, physical layer tasks are assigned to the DSP or FPGA according to their processing requirements. Computationally intensive symbol rate computations, such as modulation, are assigned to the FPGA. The DSP chip handles other tasks that are performed over a number of slots, such as average channel estimation, burst formatting and demodulation.

With both the raw processing power and flexibility of reconfiguration that the ASPE affords, it is possible to emulate multiple MSs operating on multiple carriers using a single ASPE. To determine the upper limit to the number of carriers that may be simultaneously emulated, the maximum data rate per carrier is computed. An 8-phase shift keying (8-PSK) modulated burst carries 348 data bits (116 symbols at 3 bits per symbol [1]). Given a time-division multiple access (TDMA) frame rate of 4.62 ms, in which there are eight slots, the bit rate per slot is calculated to be 75.4 kbit/s. Thus, the maximum raw bit rate, when all eight slots are occupied, is 8×75.4 kbit/s = 603.2 kbit/s. However, since channel decoding will be performed in the PC card, it may be necessary to transmit soft information and this will increase the data rate by a factor of two to four. Given that the half duplex bandwidth of the USB link is 5 Mbit/s, the ASPE is able to support the simulation of up to two carriers, each using all eight slots. These 16 slots may represent two Class 18 MSs each using 8 slots, 16 MSs each using a single slot, or any combination of multi-slot MSs using 16 slots in total.

2.4 The RF Module

The design of the RF module is strongly influenced by the ASPE configuration, particularly with respect to the implementation of frequency hopping. Figure 3 shows how the ASPE and RF module might be arranged when 8-PSK modulation is employed and two carriers are generated simultaneously. Frequency hopping is facilitated by a digital local oscillator (LO) and mixer combination within the ASPE FPGA, which upconverts the coded symbols to within the baseband bandwidth of the DACs. Since it is most convenient for the DAC sample rate to be an integer multiple of the symbol rate and the maximum DAC sample rate is 32 MSample/s, a convenient sampling frequency is 26 MSample/s. This sets the maximum frequency band over which hopping can occur to 26 MHz.

To allow independent frequency hopping of each emulated mobile, it is clear from Figure 3 that there must be as many frequency hopping stages as there are carriers. In practice, it is possible to double the internal clock rate of the FPGA and thus share the modulator between the two emulated carriers. By implementing frequency hopping within the baseband stages, the RF stage is simplified to a quadrature modulator and a RF local oscillator, which sets the frequency band of operation but does

not need to be capable of fast switching. In further stages of the RF module, amplification and gain control functions are provided to facilitate the necessary power control to comply with TS05.05 [3].

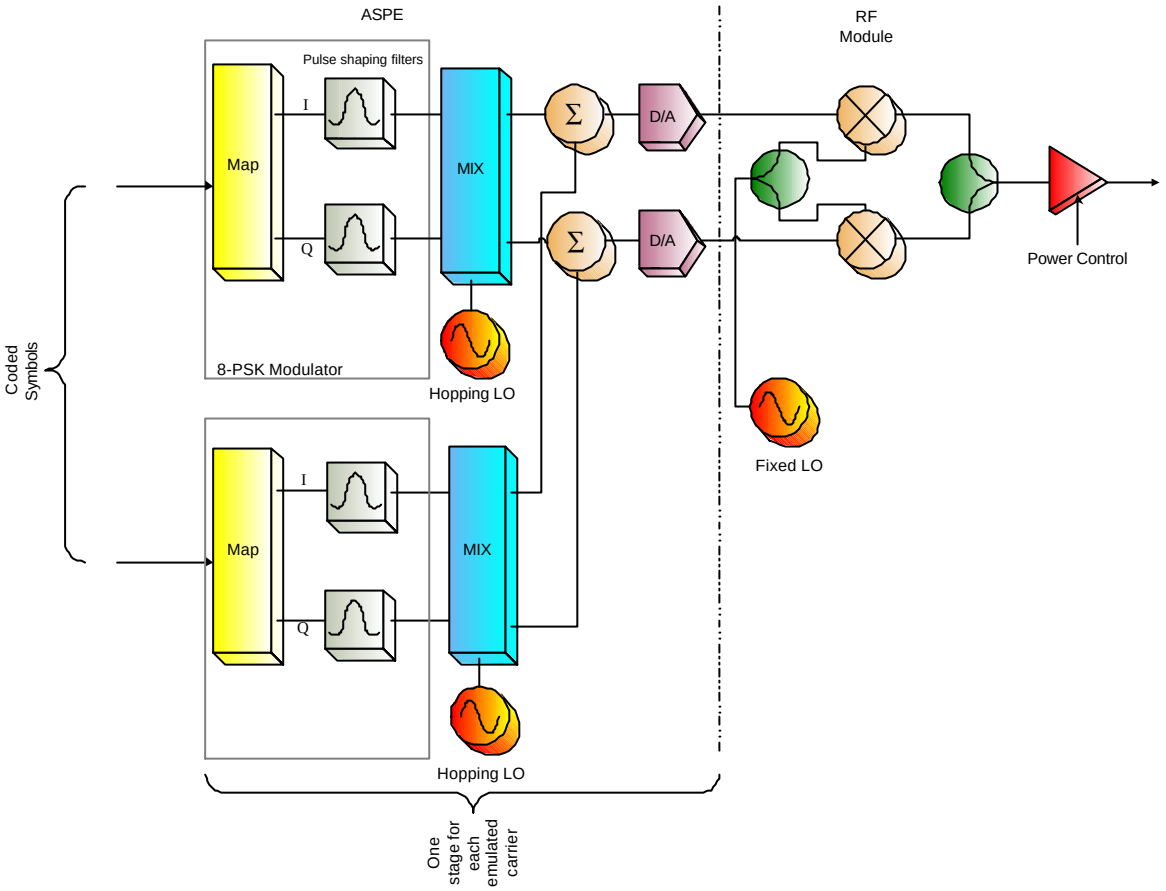

Figure 3 Implementation of frequency hopping for one emulated EDGE mobile. Functionality on the left of the dashed line is provided by the ASPE, and to the right, by the RF module.

3. Conclusions

This paper has shown that a novel reconfigurable radio architecture can be used to facilitate the emulation of up to 16 EDGE mobile stations. The hardware for implementing the physical layers and interfacing with the LSU forms a RFBBM, and consists of a PC card, an ASPE and a RF module. The functionality of each constituent part has been described, and performance has been estimated when appropriate. The combination of a reconfigurable RFBBM and a LSU has been shown to form a high performance tool for the testing of EDGE base stations, whilst its reconfigurable nature provides an highly flexible platform in which the functionality can be extended, as and when required.

Acknowledgments

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References

[1] 3GPP TS05.01: “Digital cellular telecommunications system (Phase 2+); Physical Layer on the radio path; General description (Release 1999)”. Version 8.6.0 November 2001.

[2] 3GPP TS05.03: “Digital cellular telecommunications system (Phase 2+); Channel coding (Release 1999)”. Version 8.6.0 January 2001.

[3] 3GPP TS05.05: “Digital cellular telecommunications system (Phase 2+); Radio Transmission and Reception” . Version 8.7.1 November 2000.