High-throughput, Self-routing, Optical Switch for Photonic Slot Routing

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Abstract: A high-throughput, self-routing, optical switch with low latency performance and no-contention property is proposed for the optical packet switching scheme known as photonic slot routing. The proposed switch, based on a modified Data Vortex structure, eliminates the need to pre-arrange the photonic slot transmission in a non-blocking manner, thus increasing the network bandwidth. Electro-absorption modulator technology is experimentally shown to be a promising solution for implementing compact and fast-speed operation Data Vortex switches.

1 Introduction.

Photonic slot routing (PSR) is an optical packet switching concept proposed as a cost effective and scalable alternative to wavelength routing [1]. In a PSR network, multiple packets simultaneously transmitted on different wavelengths constitute a photonic slot that is routed as a whole entity throughout the PSR network. Contrary to wavelength routing , packets on different wavelengths are not switched individually and packet switching is insensitively done with respect to the wavelength. Thus, the number of hardware resources at the PSR switching nodes is independent of the total number of wavelengths, and insensitive optical technology is deployed instead of sensitive optical devices, decreasing in this way the complexity and cost at the switching nodes. This paper presents a switching node architecture, based on a Data Vortex configuration, able to route the photonic slots arriving at any input port to any output port in a non-blocking way without the need to pre-arrange the photonic slot transmissions. The proposed novel Data Vortex switch maintains the attractive features of the original Data Vortex, having intrinsic self-routing mechanism and a simple and self control that avoids a central external control. In addition, the new mode of operation introduced makes the original switch much more efficient. improving remarkably the latency performance, resolving contention at the output and making the switch much more attractive for a compact realization.

2. Generic Data Vortex.

The Data Vortex packet switch consists of small units, called nodes, placed on a collection of concentric cylinders. Each node is positioned on a certain cylinder, on a specific height of that cylinder and at a certain angle of the virtual ring on which they are placed (see Fig.1). In this structure, packets enter the switch by the nodes of the outermost cylinder and are routed synchronously following a binary tree fashion, hopping between nodes through the physical connections lines, towards the nodes of the innermost cylinder via which they exit. An asymmetric I/O operation mode, in which a fraction of the input ports per height is used and every output node on the same height has the same destination address, is considered for better performance. Fixed-length packets are processed in a synchronous, time-slotted, and parallel manner at the nodes. In a given clock cycle the slots can hop either to a node of the next inner cylinder, moving forward within the structure, or to another node placed in the same cylinder, in order to get properly routed or in order to resolve contention. Fig.1 shows the routing of a slot whose target output is height h=11. For the correct operation of the synchronous mechanism deployed, the slots have to be processed by only one node in a given clock cycle. The connection lines must have a length equivalent to the slot duration α, in order that a slot does not reach the next node until it has been switched entirely by the previous one. Thus a generic Data Vortex adds a latency of α

per hop. For a detailed explanation of Data Vortex architecture we refer to [2].

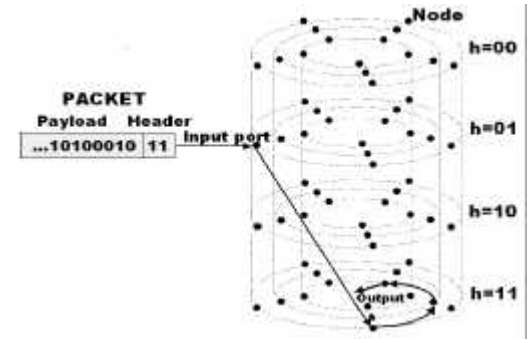

Figure 1: Data Vortex Switch Structure.

3. Improved Data Vortex.

We propose a novel Data Vortex configuration in which:

1. The total distance between two consecutive input ports on the same height is equivalent to the photonic slot duration α. As a result, the connection lines have a length that adds a latency equivalent to α divided by the number of angles K of distance. In particular, we propose to use only one node per height as input port, thus K is the total number of nodes per height. As a consequence, one slot is processed within the structure by several nodes at the same time.
2. The input ports on the different heights are aligned at the same angle position. It results in the fact that two slots arriving at two nodes which are at the same angle position arrive in the same clock cycle. We will refer to it as angle alignment.
3. The nodes of the innermost cylinder send control messages to the nodes of the next outer cylinder (in accordance with the conventional Data Vortex operation) to signal a 'busy' state until a slot completely exits the innermost cylinder.

Feature number 2 guarantees the Data Vortex correct operation although the slots are processed by several nodes at the same time, in a given clock cycle. When a slot arrives at a node X, it is routed and a control message is sent to a node Y at the same angle position on the outer level. Because of the angle alignment, guaranteed by feature 2, the slots that reach nodes X and Y arrive in the same clock cycle with a gap of time equivalent to the time it takes the control message to reach Y. And since the slots have the same duration, the control message that Y receives remains the same until it completes switching the packet. The switch state of each node, which depends on the control messages received , stays in the same state for the entire slot duration, avoiding packet splitting. Thus, the proposed configuration operates correctly with connection lines of a length equivalent to α/K. As a result, the latency decreases by a factor K with respect to the generic one. Besides, in the generic one, several slots can arrive at output nodes with the same address at the same time in a given clock cycle. If the output nodes with the same address are connected to the same output fiber, none of these slots will exit successfully in case that no contention resolution method is implemented. On the other hand, for the proposed configuration, feature 1, which specifies only one node per height used as input port, and feature 2, guarantee that only one slot arrives at one of the output nodes with the same address (i.e. on the same height) in a given clock cycle. This characteristic enables to implement a simple mechanism to resolve contention at the switch output. Feature 3 is precisely in charge of implementing this simple mechanism by avoiding that after a slot arrives at an output node, another slot reaches an output node on the same height in the subsequent cycles while current slot is still exiting. This mechanism does not require any additional complexity with regard to the conventional Data Vortex and takes advantage of the buffering resources of the Data Vortex structure.

4. **Simulations Results**

To demonstrate the improved operation we present simulation results for the case of a novel and a generic switch with five nodes per height A=5, and one of them used as input port A'=1 (asymmetric mode *K*=1/5). Fig. 2 shows the throughput under uniform traffic and for three different switch heights (H). The throughput of the novel has been measured only by means of the number of successful injections (injection rate [2]), since no packet is lost neither inside the structure or at the output. Whereas for the generic, apart from the successful injections, the rate of slots that exit the structure successfully has been also taken into account. The proposed Data Vortex configuration has a better throughput due to the output contention resolution mechanism. Although the mean number of hops that slots perform to exit the structure increases, the latency remains remarkably smaller in comparison to the generic one (40-50% less, under maximum load for the different heights), since each hop adds a latency five times smaller.

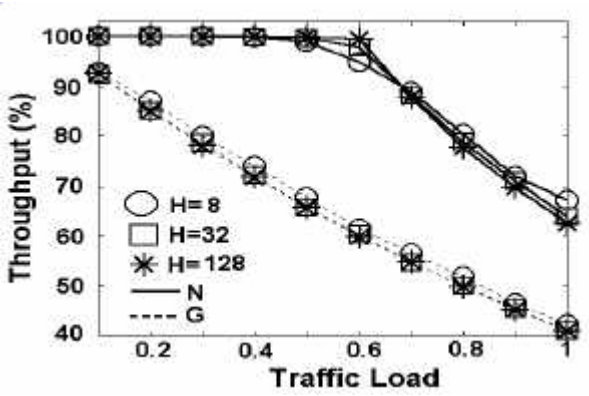

Figure 2: Throughput of the novel (N) and generic (G).

5. Data Vortex implementation.

Each slot entering a switching node is switched to a node of the same cylinder or to a node of the inner cylinder. The use of electroabsorption modulators (EAM) is proposed as an efficient and promising technology for implementing these switching nodes Thus, for implementing the 1x2 switches of each switching node, two EAMs are arranged so that the output of one of them is directed to the node of the same cylinder whereas the output of the other is directed to the inner cylinder. Both receive the entering slot and are controlled in such a way that while one of them let pass the optical signal the other absorbs it. Thus, one of the EAM is driven by the inverted driven signal of the other. Experimentally we have demonstrated the use of this technology for photonic slot routing. A WDM photonic slot is emulated by modulating three wavelengths at $\lambda 1$=1549.15 nm, $\lambda 2$=1550.78 nm and $\lambda 3$=1557.25 nm at 10 Gbit/s by using an external amplitude modulator. After the amplitude modulator, these three channels are amplified by an EDFA and fed into an electro-absorption modulator (EAM). Fig. 3 shows the power spectrum of the three channels, before entering the EAM and after the EAM when a reversed bias of 0 and −5 V is applied to the EAM. For a reversed bias of −5 V, the three channels, spaced 8.1 nm, are gated with an extinction ratio of 24 dB with a variation of only 0.5dB among the channels. Subsequently, the three channels are simultaneously gated at a speed of 78.125 MHz to emulate packet switching of packets 64 ns long by electronically controlling the reverse bias voltage of the EAM between 0 and −5 V. The eye pattern of the gated channels was wide open and for an input extinction ratio of 12 dB we measured an extinction ratio of 13.3 dB after the gating by the EAM. Gating operation of EAM has been demonstrated at more than 40 Gb/s[3]. However, for the Data Vortex switch operation the relevant parameter is not the high speed of the gating but the capability of gating simultaneously a wide WDM window enough to cover a photonic slot. We show successfully gating over a window of 8.1 nm, though EAM has the potential of gating over a wider window, ca 20

nm [3]. EAM technology is a promising candidate to build modular Data Vortex switches due to its prospect of integration. Moreover, EAM introduces low chirp and lower noise compared to proposed SOA and LOAs technologies [4].

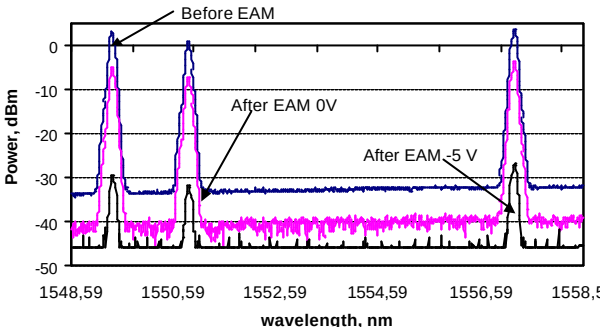

Figure 3: Power spectrum of three WDM channels at 10 Gb/s gated by using EAM.

6. Conclusions.

We have presented a novel Data Vortex switch that suits perfectly the needs of the router nodes in PSR networks. The novel Data Vortex switch operation performs the slot routing in a non-blocking manner, without any kind of contention under any kind of traffic with any offered traffic load, and without the need to prearrange the photonic slots transmissions. We have shown how the new operation mode allows the use of shorter physical connection lines, improving remarkably the latency performance, and in addition resolves the contention at the output, resulting in a significant better throughput. Furthermore, the proposed switch, due to its shorter connection lines, results attractive for a compact realization in WDM/TDM optical packet switches for telecom and supercomputing applications. Finally we have presented the use of EAM as a promising technology for implementing modular Data Vortex switches.

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