Effects of Decoding Depth on the Performance of the Modified Feedback Decoding Algorithm for Convolutional Codes

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Abstract: This paper presents further system level simulation results on the coding performance of the modified feedback decoding algorithm (MFDA) for various rate-1/2 convolutional codes and decoding depths. Results show that the MFDA compares very favourably to a best-state implementation of the Viterbi algorithm (VA), thus requiring only a decoding depth of about three to four times the constraint length of the code. However, unlike the VA, the MFDA may be realized using almost entirely analogue circuits. This offers the potential for the construction of low-power, low-complexity decoders for portable systems with moderate data rate requirements.

1 Introduction

Convolutional codes [1] are a type of error correcting code widely used in digital communication systems, especially in applications with very noisy channels. Examples with noisy environments are satellite communications and digital mobile telephony [2, 3]. These codes are characterized by two parameters depending on the encoder structure: the *code rate k/n*, which expresses the input bits per coded symbols and the *constraint length K*, which defines the memory order of the encoder. The most commonly employed decoding technique for convolutional codes is the *Viterbi algorithm* (VA) [4]. It theoretically performs *maximum-likelihood* decoding and in addition to convolutional decoding is also used in applications requiring optimum estimation of a digital sequence [5]. Practical realizations of a Viterbi decoder (VD) generally employ software or digital hardware, depending on the data rate requirements of the application [3], [6], [7]. More recently mixed-mode analogue/digital VDs have been reported which outperform their digital counterparts in terms of size, complexity, power dissipation and, in some cases, decoding speed [5], [8]. However, the need for digital path memory accounts for as much as 50 % of the total die area in a high-speed digital VD [7]. This limits further reductions in size and power dissipation using the mixed-mode approach.

An alternative approach, the *modified feedback decoding algorithm* (MFDA) proposed in [9], does not require any digital path memory, and thus lends itself to implementation using almost entirely analogue circuits. As a result, a convolutional decoder may be constructed that is smaller and dissipates much less power than a digital or mixed-mode VD. This is very important in applications where size and power consumption are of prime concern. Although, the MFDA is derived from the *feedback decoding algorithm* [10], it can be more accurately described as a modification of the VA, since it employs its path elimination mechanism.

In this paper, the coding performance of the MFDA is further investigated to establish the *minimum* decoding depth required for negligible loss in coding gain to occur. System level simulations for three optimum, rate-1/2 convolutional codes ($K = 3$, 4 and 5) show that the MFDA compares very favourably to a *best-state* VD (BS-VD) and hence, the required decoding depth need only be between $3K$ and $4K$. This is a very important advantage in the case of the MFDA since a reduction in the decoding depth minimizes the internal dynamic range requirement of the decoder resulting in additional savings in size and power dissipation.

2. Viterbi Decoder (VD)

A simplified functional block diagram of a BS-VD is shown in Fig. 1. This type of implementation provides an optimum maximum-likelihood VD in practice. The decoder consists of the branch metric computer (BMC), add-compare-select (ACS), storage survivor memory (SSM) and the output decision (OD) blocks. The difference between BS-VD and the more practical *fixed-state* VD (FS-VD) is the extra OD block.

The function of each decoder block is as follows. The BMC calculates the *metrics* of each trellis branch (using squared Euclidean or Hamming distance) between the received noisy symbols and the

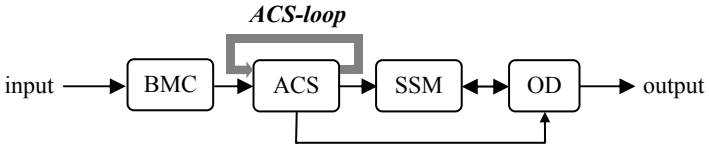

Fig. 1: Block diagram of a BS-VD.

corresponding branch symbols. Given the branch metrics, the ACS computes a new set of *path metric*s entering each state at each time-step. It then selects the *survivor* path for each state and updates the SSM accordingly. The digital SSM block stores the history of the survivor paths at each time-step in a hypothetical digital representation. The size of this digital memory is determined by the depth of the decoding window L in the trellis, and thus the value of L is of prime importance. For optimum maximum-likelihood decoding the ideal case of infinite L is assumed. In practice, simulations have shown that a value of L about $5K$ for a FS-VD results in negligible loss of coding gain [2]. However in the case of a BS-VD, an L of $3K$ to $4K$ is sufficient to avoid any appreciable loss in coding gain [11]. This is because of the extra OD block, whose role is to choose the state with the maximum metric at the end of each decoding cycle (L time-steps); unlike a FS-VD that always selects in random a pre-determined state [5], [8]. The OD block may be viewed as a winner-take-all (WTA) network [12]. In practice, the hardware complexity of the OD block increases exponentially with K which makes it impractical for $K > 4$.

3. Modified Feedback Decoder (MFD)

The MFDA [9] splits the trellis diagram into two sub-trellises. The novelty behind this approach is that there is no need for digital path memory since the decoded output is determined by a simple decision as to where the selected path originates (upper or lower sub-trellis). The decoding decision is then fed-back and the sliding block (window of depth L levels) advances one time-step ahead splitting the selected trellis over again.

The general block diagram of a MFD is shown in Fig. 2. The symbol storage (SS) block stores a window of depth L (sliding block) of the received sequence to be processed by the BMC and ACS blocks. In the MFDA modified trellis there are 2^K states, which is twice that in a VD for the same K. This means that two identical ACS blocks must be used in parallel for both sub-trellises. Nevertheless, the complexity of the ACS block in a MFD is less than that in a VD because there is no need to update any digital path memory.

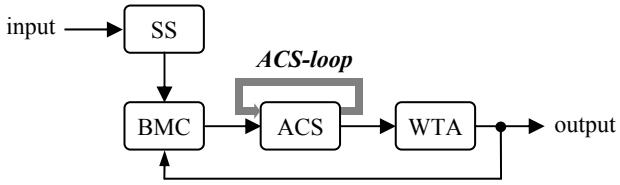

Fig. 2: Block diagram of a MFD.

At the end of each decoding cycle when a complete sliding block has been processed, it is necessary to determine whether the path with the maximum metric lies in the upper or lower sub-trellis. This is done by the WTA block whose output decision also updates the BMC by means of feedback. In fact, the WTA output determines the beginning state of the next decoding cycle while still having an effect on the next $K - 1$ trellis levels. This means that in the BMC the branch symbols on the first $(K - 1)$ levels are variable depending on the $K - 1$ previous decoded bits. Finally, in each decoding cycle the first K levels of the modified trellis are processed in parallel, where no path elimination is required.

4. Simulation Results

In order to investigate the effects of L on the coding performance of the MFDA and to allow direct comparison with the VA (i.e., BS-VD and FS-VD), an encoder-decoder model was generated and

simulated using Simulink blocks. The Simulink models were converted into *C* code using the Real-Time-Workshop. This enabled complete decoders up to and including $K = 5$ to be investigated. Antipodal signalling in an AWGN channel was employed and the input signal to the decoders was not quantized.

Figures 3 to 5 show plots of BER against E_b/N_o for these decoders for various values of L (MFD and BS-VD). The FS-VD truncated to $L = 6K$ is also included in the graphs. From these plots it becomes apparent that the MFD can achieve a similar BER performance to the FS-VD but for smaller values of L ($< 4K$). Also the loss of coding gain of the MFD compared to the corresponding BS-VD is less than 0.04 dB for $L = 6K$ and less than 0.1 dB for $L = 4K$. These losses are negligible considering the benefits of size and power dissipation offered by the MFDA approach. The optimum value of L for the MFDA is therefore between $3K$ and $4K$.

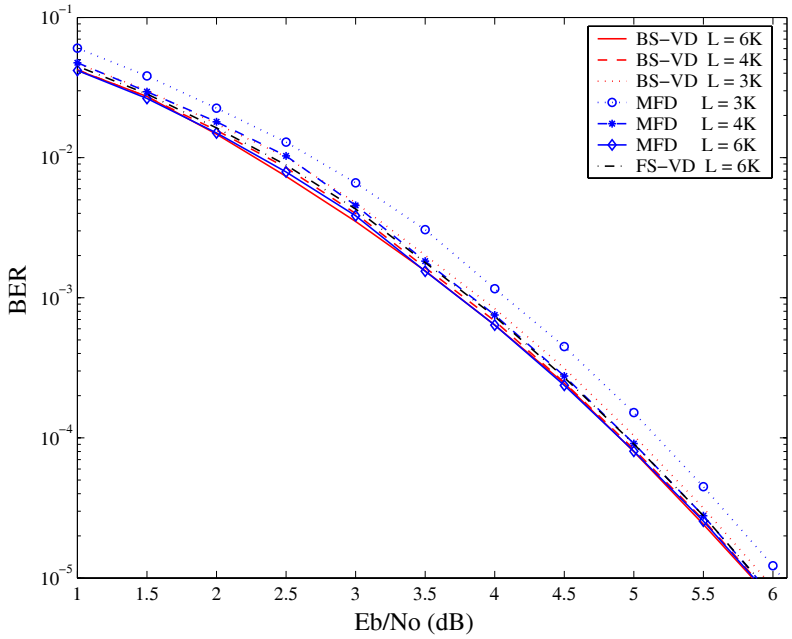

Fig. 3: Coding performance for the $K = 3$ code (code generators: 111; 101).

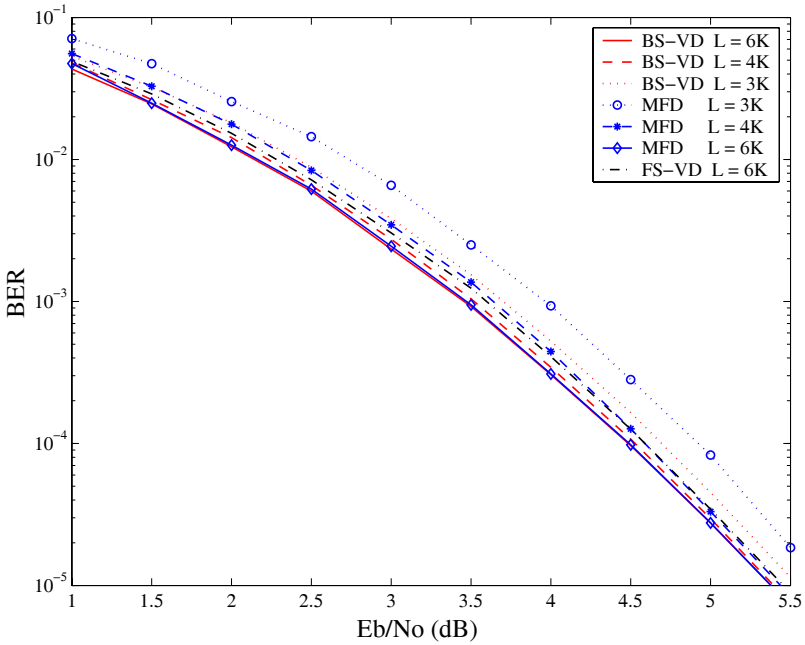

Fig. 4: Coding performance for the $K = 4$ code (code generators: 1111; 1101).

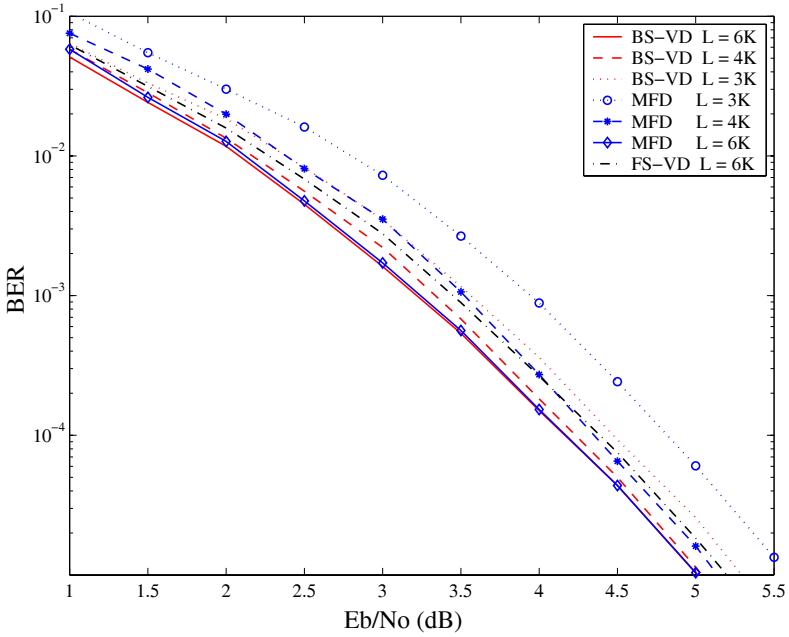

Fig. 5: Coding performance for the $K = 5$ code (code generators: 11101; 10011).

5. Conclusion

Using computer simulations, the coding performance of the MFDA has been compared with that of the VA (FS-VD and BS-VD implementations). Results show that a similar coding performance to a FS-VD may be achieved by a MFD with a smaller decoding depth. Furthermore, a MFD compares very favorably to a BS-VD, requiring a decoding depth between $3K$ and $4K$. A MFD may be constructed using almost entirely analogue circuits of low complexity making it suitable for low-power portable applications of moderate data rates.

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