Cascade Hadamard based Parallel S? Modulation for Software Radio

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Abstract: The weakest point in the development of versatile Software Radio is the Analog-to-Digital converter, as very high performance is needed to transform RF or IF signals. Sigma-Delta (S?) converters are a good approach but they are limited primarily by the stability and the oversampling necessary to achieve a high resolution. In this paper we present a new hybrid S? converter that because of the characteristic strengths of each of the modules that comprises it, makes it a very attractive architecture to attack these two problems.

1. Introduction.

Two important S? based architectures are cascade and parallel modulators.

The 1-1 cascade S? is a modulator that obtains the same results as the second order S? but with a more stable structure. (1) shows the ideal expression for the theoretical architecture.

$$Y(z) = X(z) - (1 - z^{-1})^2 \cdot E(z) \qquad (1)$$

X(z), Y(z) and E(z) are the z-transforms of the input, output and quantization error respectively [1, Chapter 6].

With S? modulators a significant restriction is imposed by the oversampling to achieve by good resolution. The parallel architecture with Hadamard modulation solves this problem by encoding each of m samples with a Hadamard orthogonal code, m being the number of branches. Doing this it is possible to pass the signal plus error through a filter and then demodulate the signal to its pre-filtered state. Hence, as shown in (2), the error is filtered and the signal passes intact, removing the in-band noise.

$$Y(z) = \sum_{i=1}^{m} \left[H(z) \cdot E_i(z) \cdot (1 - z^{-1}) \right] * U_i(z) \cdot z^{-k} + X(z) \qquad (2)$$

X(z) and Y(z) are the z-transforms of the input and output respectively, $E_i(z)$ the z-transform of the quantization error of the S? modulator in branch i, $U_i(z)$ the z-transform of the Hadamard sequence in branch i and k the delay caused by the filter H(z), due to its special characteristics [2,3,4].

2. Cascaded Parallel Structure.

2.1. *Architecture*

This structure is similar to the one suggested in [5], in which a time-interleaved architecture was placed in the second stage. The structure presented in this paper uses a Hadamard parallel architecture in the second stage and is depicted in Figures 1 and 2. The reasons for putting the parallel structure in the second stage are simplicity and error rejection. In the next section it is demonstrated that the Digital Cancellation Filter is very simple and easy to obtain. Errors resulting from component mismatches, which are expected to occur in parallel architectures, are less influential in a cascade S? modulator [1, Chapter 6] if they appear in the second stage.

2.2. *Digital Cancellation Filter.*

The Digital Cancellation Filter is calculated from the expressions of the two different structures as it is done for the 1-1 cascaded S? modulator.

$$Y(z) = Y_1(Z) + F(z) \cdot Y_2(z); \quad F(z) = -\left(1 - z^{-1}\right);$$

$$Y(z) = \sum_{i=1}^{m} \left[H(z) \cdot E_i'(z) \cdot (1 - z^{-1}) \right] * U_i(z) \cdot z^{-k} \cdot F(z) + X(z) \qquad (3)$$

(3) shows that the quantization error resulting from the Parallel Structure, is filtered and shaped in second order, whilst it does not affect the signal.

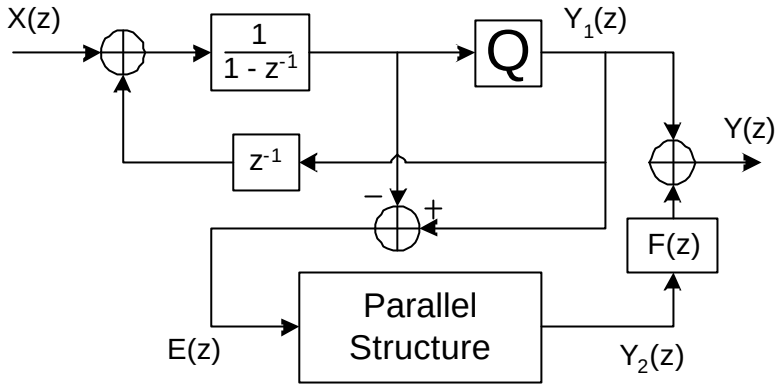

Figure 1. Cascaded SD Modulator with Parallel second Stage.

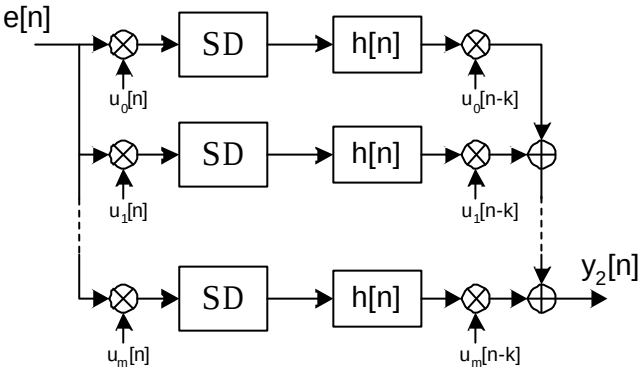

Figure 2: Details of parallel structure from Figure 1

2.3 *Limitations.*

This second order shaping of the quantization error typical of the parallel structure does not offer good performance in all cases.

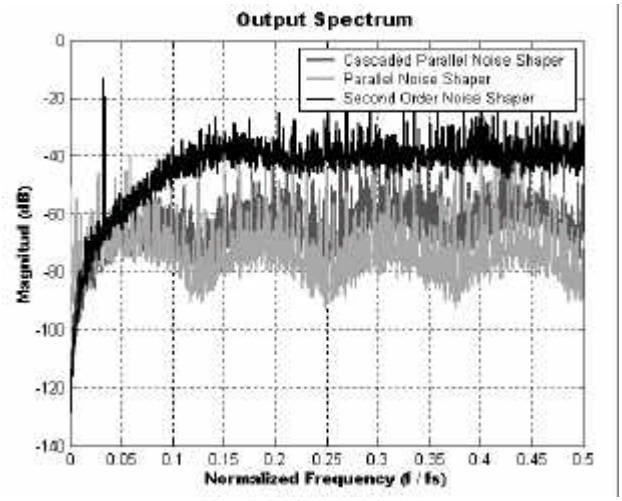

Figure 3. Periodogram of the output for the proposed architecture, the cascade and the parallel S? modulators.

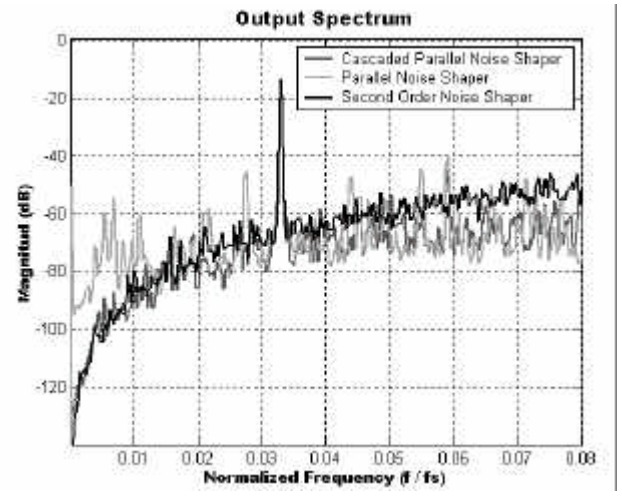

Figure 4. Zoom in the low frequencies of Figure 3.

Looking the shape of the noise in each case (figure 3) and noting that the error that affects the signal is the integration of the error from DC to the sampling frequency divided by two times the oversampling ratio (2*OSR), it is obvious that depending on the OSR the cascaded parallel structure studied is not always the best solution. In one extreme, not having any oversampling, the noise integrated will be from DC to $f_s/2$, which means that the best performance will be given by the parallel S? modulator, as it has flattened noise throughout the spectrum. In cases having a large OSR the best solution will be the cascade with its second order shaping of the noise, as in the lower frequencies the noise goes below that achieved by the cascaded parallel implementation, whilst the simple parallel does not have the characteristic noise shaping of S? modulators near DC (figure 4).

Therefore, there is a certain range of the OSR in which the performance is better producing a stable structure that does not need as much oversampling as the cascade S? modulator (as shown in figure 5), relaxing one of the most important characteristics of S? converters that makes it impossible to convert RF signals.

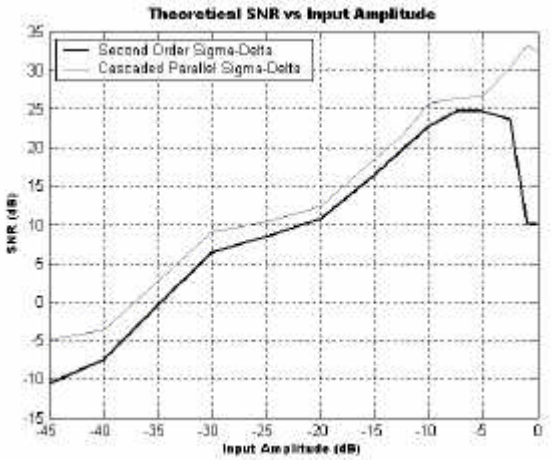

Figure 4. Dynamic Range plotfor the proposed architecture and the Second Order S? ADC.

3. Conclusions.

We have studied a novel hybrid architecture that relaxes the performance requirements of both structures which comprises it. Less oversampling ratio is needed than the second order S? modulator to achieve the same SNDR; and it is more stable than the parallel structure because this component is placed in the second stage of the cascade [1, Chapter 6]. The drawback of this hybrid is that there exist some ranges of OSR in which its performance is marginally inferior to the existing implementations, though its performance is generally superior.

References.

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[5] X. Wang, W. Qin & X. Ling, "Cascaded Parallel Oversampling Sigma-Delta Modulators", IEEE Trans. Circuits Syst. II, Vol 47, No 2, Feb 2000, pp. 156-161.