Intermodulation Investigation of Fractional-N Frequency Synthesiser

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Abstract: This paper discusses how intermodulation effects in fractional-N synthesisers influence the spectral purity, causing discrete spurious components. The analysis is proved both in simulation and in measurements of real circuits. An ADS model of fractional-N synthesiser is also provided for further work, by which the intermodulation can be simulated at the circuit level.

1. Introduction

Phase-locked Loops(PLL) are widely used in the area of frequency synthesis. In a PLL, the VCO output frequency f_{vco} is determined by the reference frequency f_{ref} and the division ratio N, such that

$$f_{vco} = N * f_{ref} \tag{1}$$

In conventional frequency synthesisers, the division ratio N is integer. To achieve fine frequency resolution, small reference frequency and tight loop bandwidth are needed. But tight loop bandwidth will cause longer switching times and less suppression of VCO phase noise.

Fractional-N frequency synthesisers, shown in Fig.1(a), can achieve finer frequency resolution than the reference frequency. Dual-modulus prescaling technique is used to implement the fractional divider in the frequency synthesiser. In fractional divider, the division ratio is periodically altered from N to N+1. So the average VCO output frequency is

$$\begin{aligned} average f_{vco} &= \frac{1}{T_N + T_{N+1}}[T_N * N * f_{ref} + T_{N+1} * (N+1) * f_{ref}] \\ &= [N + \frac{T_{N+1}}{(T_N + T_{N+1})}] * f_{ref} \\ &= (N + x) * f_{ref} \end{aligned} \tag{2}$$

Where T_N is the time that the divider is dividing by N and T_{N+1} is the time that the division ratio is N+1. x is the fractional portion of the average division ratio [1].

Fractional-N frequency synthesisers have discrete spurious components which affect the spectral purity. In a fractional-N frequency synthesiser, because of the fractional division ratio, the frequency of the VCO output signal and the frequency of the reference frequency are non-harmonically related. The intermodulation of these non-harmonically related frequencies will potentially cause discrete spurs.

2. Analysis of the intermodulation model

A model of fractional-N frequency synthesiser with a VCO cross coupling path is shown as Fig.1(b). Apparently, there are two principal frequencies in the loop, the reference frequency

f_{ref} and the VCO output frequency f_{vco}. Due to the fractional division ratio, these two frequencies are not harmonically related. When they present at a point simultaneously, intermodulation may result.

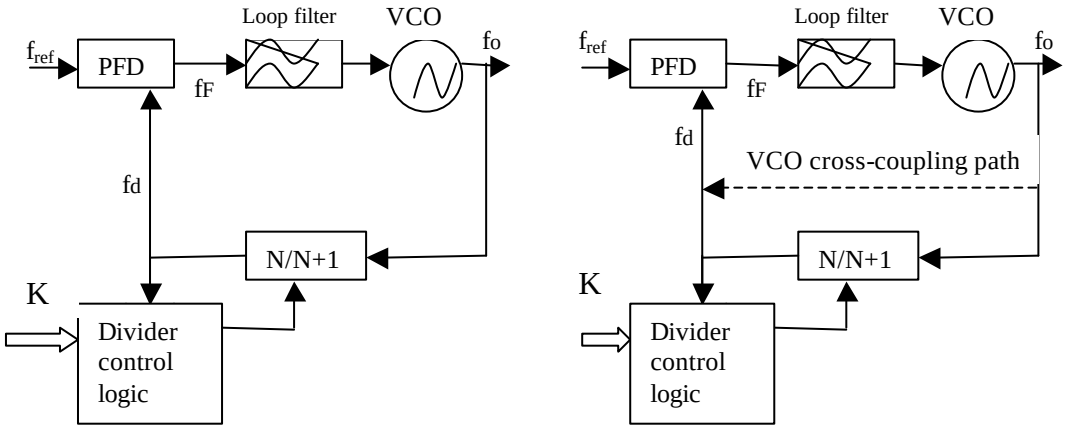

Fig.1 *structure of fractional-N synthesiser.*
(a) basic arrangement; (b) with a cross coupling path

A possible cross-coupling path is shown in Fig.1(b), [2]. With this path, the VCO output signal will present at the point of the output of divider, resulting in the divider output signal f_d. From equation (2), f_d is given by

$$f_d = f_{ref}(m \pm n(N+x)) \tag{3}$$

where m and n are integers. Then, the output of the phase/frequency detector(PFD), f_F, is given by

$$f_F = f_d - f_{ref} \tag{4}$$

Using (3) into (4), we can write

$$\begin{aligned} f_f &= f_{ref}((m \pm nN - 1) \pm nx) \\ &= f_{ref}(M \pm nx) \end{aligned} \tag{5}$$

Because the phase/frequency detector aliases all frequency components to the range [$-f_{ref}/2$, $f_{ref}/2$], then (5) reduces to

$$f_f = f_{ref}[nx - round(nx)] \tag{6}$$

From (6) we know, the number of unique intermodulation frequencies, p, depends on the fractional part of division ratio, and p should satisfy

$$px = integer \tag{7}$$

This analysis can be proved by a practical model [2]. Considering the VCO cross coupling path in Fig.1(b), the adding of the divider output signal and the VCO output signal, coming from the cross coupling path with a relative amplitude A, will cause a timing jitter, $?t(n)$, which is shown as Fig.2. It can be expressed as

$$\sin(2p\Delta t(n)/T_{ref}) + A\sin[2p\,k(n+\Delta t(n)/T_{ref})] = 0 \qquad (8)$$

Analysing (8) in Matlab with a realistic PLL design, where the reference frequency is 20MHz, the natural frequency of the loop is 250KHz, the division ratio is 90.46 and relative amplitude *A* is -40dB, we can clearly find the intermodulation spurious components illustrated in Fig.3.

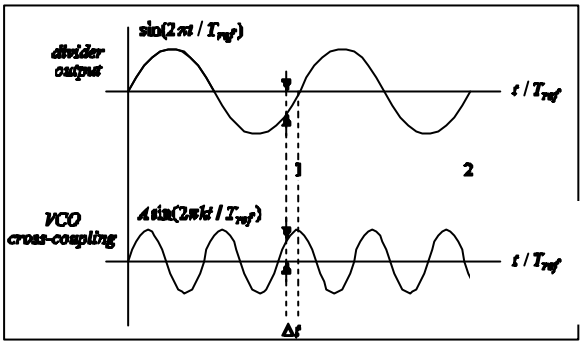

Fig.2 *Effect of VCO cross-coupling onto frequency divider output*

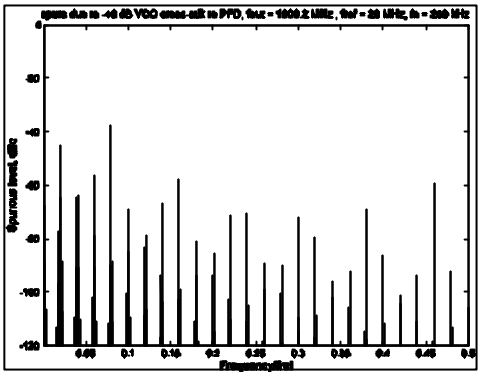

Fig.3 *discrete spurious components due to -40dB VCO cross coupling onto divider output, f_{vco}=1809.2 MHz, f_{ref}=20 MHz, division ratio=90.46*

Fig.4 is the measured SSB phase noise performance taken from real PLL circuit that used the same synthesiser digital dividers and PFD driven firstly in integer-N mode with division ratio 25 and then by a simple first-order sigma-delta fractional-N PLL with division ratio 25.58 [3]. In Fig.4 we can clearly find those discrete spurs in the phase noise spectrum when the division ratio is fractional value.

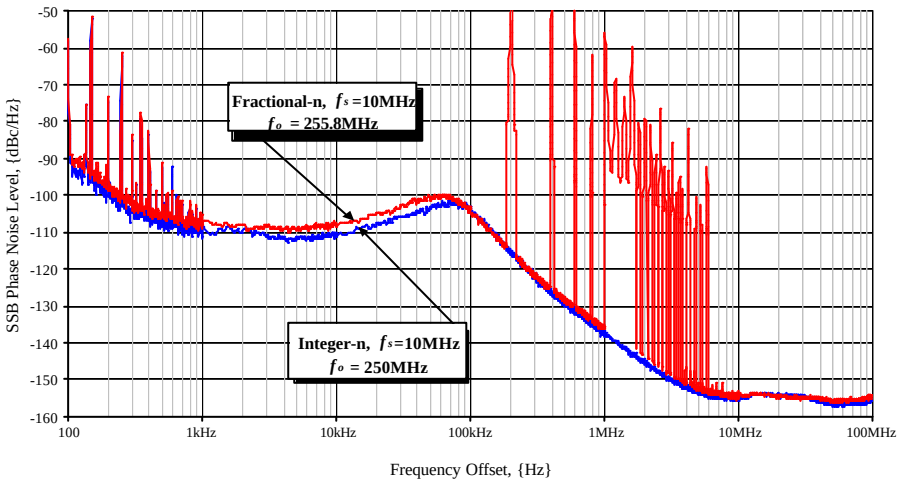

Fig.4 *measured phase noise for a integer-N mode synthesiser and a first-order sigma-delta fractional-N synthesiser, with f_{ref}=10 MHz, loop natural frequency=100KHz, integer division ratio=25 and fractional division ratio=25.58.*

3. An ADS model of Fractional-N frequency synthesiser

Fig.5 is a circuit level model of fractional-N frequency synthesiser built in ADS. The whole loop consists of a phase/frequency detector, a third order type II loop filter with natural

frequency 250 KHz and a VCO with built-in fractional divider. The PLL loop is designed suitable for digital cellular system (DCS) base station applications. The reference frequency is 20 MHz and the division ratio is 90.46, so the VCO output frequency is 1809.2 MHz.

The VCO component in this model is combined with a fractional divider, with an input port for division ratio control, which can be connected to the bitstream generated by a control logic, such as sigma-delta modulator. The setting up of VCO output frequency is shown as Fig.6.

For the simulation of investigating intermodulation effects, a summer will be added to the model, connecting the VCO output signal to the divider output signal as the VCO cross coupling path, and an amplifier will be used to achieve the relative amplitude of the cross coupling signal.

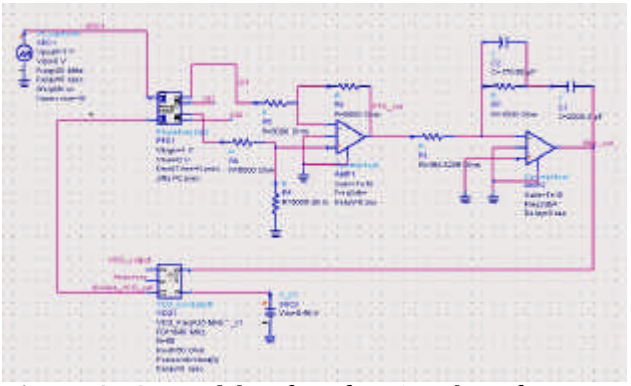

Fig.5 *ADS model of fractional-N frequency synthesiser, with f_{vco}=1809.2 MHz, f_{ref}=20 MHz, division ratio=90.46 and natural loop frequency=250 KHz*

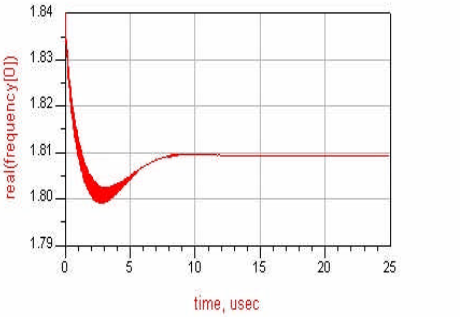

Fig.6 *simulation result of the setting up of the VCO output frequency*

4. Conclusions

From above discussion we can find out that discrete spurious components which degrade the spectral purity of fractional-N frequency synthesisers are caused by intermodulation effects existing in the synthesiser, and the number of those fractional spurs depends on the fractional portion of the division ratio.

A circuit level model of fractional-N frequency synthesiser has been built in ADS. Further research of addressing and reducing the level of those spurs can be based on this model.

5. Acknowledgements

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6. Reference

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[3] Ian Thompson, *Strategies for the Analysis and Design of a Low Noise, Frequency Agile Synthesiser*, PhD thesis, UCL, May 2003.