A Simple Adaptive Sigma Delta Modulator for Software Defined Radio

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Abstract: In this paper we propose a simple and flexible design of analog-to-digital converter based on a single adaptable architecture of high order single loop sigma delta modulator suitable for multimode operation and adaptive wireless systems. The modulator is adaptable to operate in different signal bandwidth and signal-to-noise ratio (SNR) by varying the feedback gain values of local resonators and integrators that optimize the noise transfer function of the loop filter while also meeting the stability constraint. A capacitor array implementation is employed to generate the desirable range of gain values. It is shown by simulation that it meets the SNR and bandwidth requirements of different wireless standards such as GSM and WCDMA and provides a simple reconfigurable platform.

1. Introduction:

The concept of software radio which underpin the development of future wireless communications requires highly flexible and adaptive radio front-ends [1]. Analog-to-digital converters (ADC) are very important building blocks of digital wireless communication systems and in particular more challenging for software defined radio implementation to operate in different signal bandwidths and channel conditions. Such systems require the SNR and bandwidth to be reconfigurable while requiring minimum modification of the system hardware. Therefore a flexible ADC with the ability to adjust its design parameters for adaptive and multimode operation with efficient use of the available power is required.

Sigma delta modulator (SDM) provides very flexible architecture based on digital circuitry and trade-off between SNR and bandwidth. By varying the oversampling ratio (OSR), loop filter order, and quantizer resolution, different output SNR and bandwidth for a SDM can be achieved. Large number of research work has been carried out in this area however most of which is on designing configurable ADC to operate in different mode. For example a multimode SDM for direct conversion receiver was proposed in [2] using second order loop filter with 6-bit quantizer and multibit feedback digital to analog converter (DAC) employing dynamic element matching (DEM). This design method provides fixed noise transfer function (NTF) curves suitable for specific standards however the architecture is not flexible for adaptive type of systems.

Here we propose a different approach for the design of an ADC using highly flexible and adaptable architecture of SDM suitable for both multimode and adaptive operation referred to here as “reconfigurable”. This is also important for the development of low cost adaptive single wideband ADC platform for cellular multiuser systems in particular at the base stations. Unlike conventional SDM which concentrates on improving the SNR for a given signal bandwidth here we adapt the NTF parameters of a single architecture by varying the locations of zeros (i.e. local resonator gain values) to optimize and operate for different signal bandwidth. Similar idea of gain adaptation is described in [3] for tunable center frequency bandpass SDM. Using our approach a fine granularity of a very useful range of output SNR and operating bandwidth is obtained. This design is also shown to be beneficial for receivers adapting to fading channel conditions [4]. Below we present the proposed design method and the simulation performance results.

2. Design of Adaptable Sigma Delta Modulator:

A higher order SDM employing architecture of cascade of resonators with feedback (CRFB) shown in Figure 1 is designed.

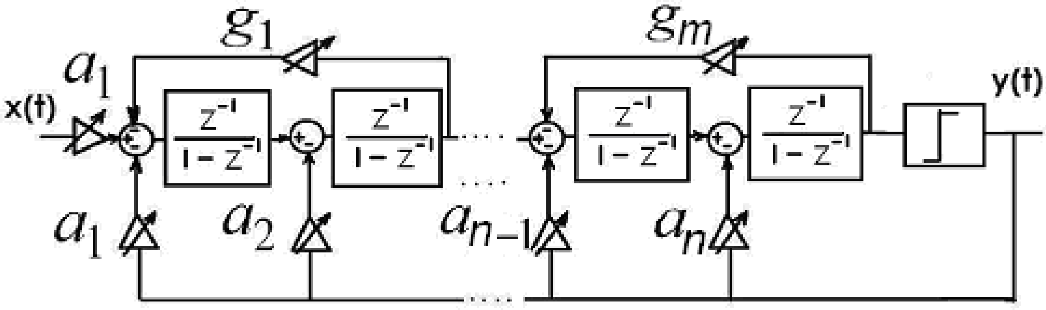

Figure 1: Model of the proposed adaptable higher order single loop SDM

The NTF of such SDM architecture can be written as:

$$NTF(z) = \frac{\prod_{j=1}^{m}((z-1)^2 + g_j)}{\prod_{j=1}^{m}((z-1)^2 + g_j) + \sum_{\substack{i=1 \\ j=1}}^{n,m}[(z-1)^{j-1}(a_{2j-1}(z-1)+a_i) \cdot \prod_{k=j+1}^{m}((z-1)^2 + g_k)]} \tag{1}$$

where n is the number of integrators and m is the number of local resonators ($m <= n/2$). The zeros of the NTF are defined by the local resonator gain values g_j and the poles are defined by the feedback gain values a_i and g_j. The modulator stability, bandwidth, and output SNR are determined by the ratio of in-band noise suppression to out-of-band gain of the NTF, which is a function of a_i and g_j. The stability constraints of higher order single loop modulator require that the lowest feedback gain value is used for the first integrator stage and increased for the subsequent stages such that the NTF value do not exceed the limit for a given loop filter order [5]. It is noted that optimum a_i can also be generated using software tools, for example Delta Sigma Toolbox [6]. Once a_i are selected, the output SNR and bandwidth of the modulator can be adjusted by varying the values of g_j, which are selected such that multiple notch frequencies $f_{notch(j)}$ are created as follow:

$$f_{notch(j)} \approx {F_s}/{2\pi} \sqrt{g_j} \ ; \qquad f_{notch(j)} \leq B \tag{2}$$

where F_s is the sampling frequency, B is the desired signal bandwidth ($B = F_S / 2R$) and R is the OSR. Although better SNR for a given bandwidth can be achieved by iteratively optimizing the NTF searching for optimum values of g_j [5], in this work however for simplicity and ease in implementation the g_j values are chosen such that the m notch frequencies are placed equidistantly within the signal bandwidth $f_{notch(j)} = jB/m$. The values of g_j can be calculated as follow:

$$g_j = \left(\frac{j\pi}{mR}\right)^2 \tag{3}$$

In the switched-capacitor implementation of the SDM, the gain values are determined by the ratio of sampling to integrating capacitors. Optimized NTFs for different signal bandwidth are obtained by using variable a_i and g_j values. This is efficiently achieved by employing arrays of p and q sampling and integrating capacitors of different nominal that form matrices of $p \times q$ gain values for each stage of the loop filter and local resonators. For example acceptable granularity of SNR range has been achieved by selecting $p=q=10$. With this arrangement g_j values ranging from 0.001 to 0.1 is generated allowing the modulator signal bandwidth to be varied from ~Fs/200 to ~Fs/20 with adequate output SNR. In the scenarios where the operating bandwidth is fixed, output SNR can be adjusted by varying the g_j values for $j<m$ corresponding to the location of frequency notches such that the condition in (2) is satisfied while keeping the last resonator gain value g_m fixed as $g_m = (\pi / R)^2$. In addition to the gain adaptation method described, by using different set of gain values the modulator can also be easily reconfigured to operate in different loop filter order.

3. Simulation Results: A system with the proposed SDM design is modeled in Matlab® and Simulink®. The loop filter order of 4 and quantizer level of 3 are used to demonstrate the design and evaluate its performance. The a_i and g_j values are selected from the matrices of gain values of capacitor arrays as described earlier. The modulator is simulated for several signal bandwidths using different g_j values while keeping the a_i fixed. Figure 2 shows the output power spectral densities (PSD) for different signal bandwidth of 2 MHz, 1.5 MHz, 1 MHz and 500 kHz sampled at 64 MHz using 65536 point FFT Hanning window.

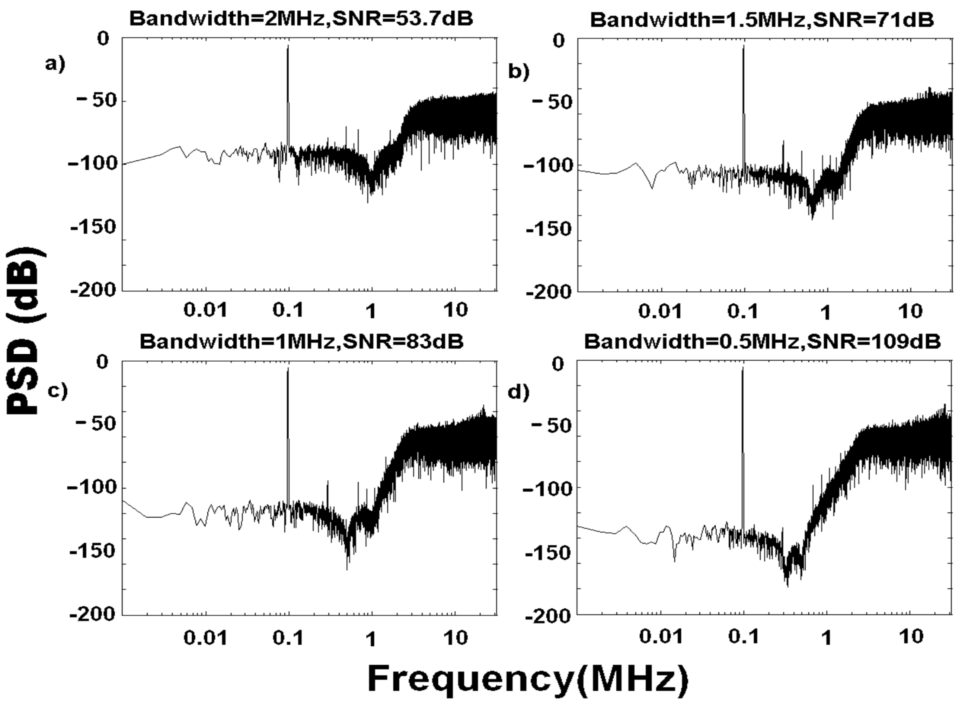

Figure 2: Output spectrum of the 4th order modulator for different signal bandwidth sampled at 64 MHz. Fixed values of a_1=0.01, a_2=0.06, a_3=0.3, a_4=0.8 are used for each case with a) g_1=0.002, g_2= 0.04, b) g_1=0.004, g_2=0.02, c) g_1=0.002, g_2=0.01, d) g_1=0.001, g_2=0.002.

It can be clearly seen that by only varying g_j values the modulator can be easily reconfigured for different signal bandwidths (e.g. WCDMA=2MHz, DECT=1.5MHz, CDMA=0.62MHz, Bluetooth=0.5MHz, GSM=0.2MHz) and meeting satisfactory SNR requirements of the standards. In addition it is shown in Table 1 that a lower order modulator could be used for a given signal bandwidth to reduce complexity and power while achieving the required SNR.

Modulator Order	a_1	a_2	a_3	a_4	g_1	g_2	**Achieved SNR**
4	0.01	0.06	0.3	0.8	0.002	0.01	83 dB
3	0.044	0.23	0.5		0.05		72 dB
2	*0.3*	*0.5*			*0.003*		*58 dB*

Table 1: Achieved output SNR with 1 MHz signal bandwidth oversampled at 32x.

4. Conclusions: A flexible architecture of high order single loop sigma delta modulator is proposed and investigated for multimode and adaptive software-defined radio systems. Capacitor array implementation to generate large number of gain values is used to meet the output performance requirements for different wireless systems. Stability of the modulator is ensured by appropriate selection of feedback gain values. The flexibility and adaptability with a single architecture are the major benefits of this modulator design. This is essential contribution leading for the development of an adaptive single wideband ADC for multiuser systems, which is the subject of current investigation.

References

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