Distributed Transversal Filter for Encoding and Decoding unipolar CDMA signals

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Abstract: A novel structure that encodes and decodes very high speed unipolar Code Division Multiple Access (CDMA) signals is proposed. This scheme is based on the analogy between the distributed amplifier and the transversal filter. By adjusting the gain of each tap and the delay between taps, the proposed device acts as a high-speed encoder (transmitter) or correlator (receiver). The theoretical analysis and the implementation using MMIC HEMT foundry process are presented.

1 Introduction

Code Division Multiple Access (CDMA) systems find many applications in wireless systems and are widely known for their asynchronous operation capacity and security. In the recent years, there has been growing interest in Optical CDMA as it is viewed as an excellent candidate to develop a new generation of Local Area Networks. The key component of the CDMA transmitter is an encoder capable of generating a high binary rate sequence. Similarly, the key component of the receiver is a correlator with ability to detect the correct sequence and ignore others. Although the structure presented in this paper can be applied to any CDMA system, the main application will be in the Optical domain because it uses unipolar codes and takes advantage of the large bandwidth provided by the device proposed.

Detailed study of the distributed transversal filter (DTF) was reported in [1] where the authors demonstrated that the distributed amplifier and the transversal filter are functionally equivalent. Since then the distributed transversal filter has been designed mainly for pulse shape applications [2] [3] [4]. Recently, work done in UCL showed that the DTF can act as CDMA encoder or decoder by setting the time delay between cells equal to the chip time and the gains according to the codeword of a specific user [5]. However, in such design, the number of stages is equal to the number of the chips in the codeword which limits the number of users. In fact, due to practical restrictions, it is impossible to build a DTF with more than a certain number of stages. This limitation means that the number of codewords with good correlation properties is small so the number of users in the network is reduced. In the structure proposed in this paper, the number of stages is equal to the number of "positive" chips. By having variable delays between stages instead of fixed, it is possible to have longer codewords for a given number of stages.

2 Theory

In general, a (n,w) code is a family of unipolar codes with length n and weight (i.e. number of "positive" chips) w. Each CDMA user is assigned a codeword (a_1,a_2,...,a_k,...,a_w) with $a_{k+1} > a_k$ and $a_k \leq n$ where each element of the array is the position of a positive chip in the sequence. The user transmits data bit "one" by sending its sequence in the time T_{bit} therefore $T_{chip} = \frac{T_{bit}}{n}$.

Figure 1 represents the reverse-mode topology of the distributed transversal filter. The delay per section is the sum of delays in the input and the output lines: $\tau_k = \tau_{gk} + \tau_{dk}$.

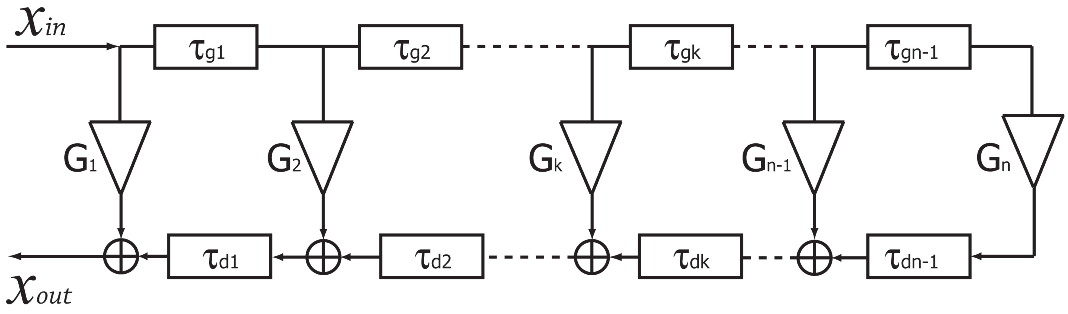

Figure 1: *Block diagram of the Distributed Transversal Filter in reverse-mode operation*

Encoder

The encoder of the CDMA system generates a fast unipolar sequence when a pulse with width T_{chip} is applied. In order to achieve that, the delay of each stage of the DTF is defined as follows:

$$\tau_k = (a_{k+1} - a_k)T_{chip} \tag{1}$$

Hence, the time-domain response of the encoder may be represented as:

$$x_{out_{ENC}}(t) = \sum_{k=1}^{w} G_k x_{in}(t - (a_k - a_1)T_{chip}) \tag{2}$$

Decoder

The decoder of the CDMA system should be able to generate a correlation peak proportional to the number of positive chips when the correct sequence is applied. In order to achieve that, the delay of each stage of the DTF is defined as follows:

$$\tau_k = (a_{w-k+1} - a_{w-k})T_{chip} \tag{3}$$

Hence, the time-domain output response of the decoder is given by

$$x_{out_{DEC}}(t) = \sum_{k=1}^{w} G_k x_{in}(t - (a_w - a_{w-k-1})T_{chip}) \tag{4}$$

One should notice that, for a given codeword, the encoder and decoder are effectively the same circuit but with the time delays τ_k and τ_{n-k+1} swapped for every k integer and $k \leq \frac{n}{2}$.

3 Implementation with MMIC

Figure 2 shows the block diagram of the Distributed Transversal Filter that is designed using the process ED02AH 0.2μm pHEMT with $f_t = 60GHz$.

The gain blocks are designed using two pseudomorphic HEMTs in cascode configuration. This is preferred over the basic common-source configuration mainly due to the higher output resistance and lower input capacitance per stage.

The inductors, used to construct the gate and drain artificial transmission lines (ATL), are designed with thin microstrip transmission lines. The inductance L_g and the input capacitance of the cascode C_{in} form an artificial transmission line (ATL) with characteristic impedance

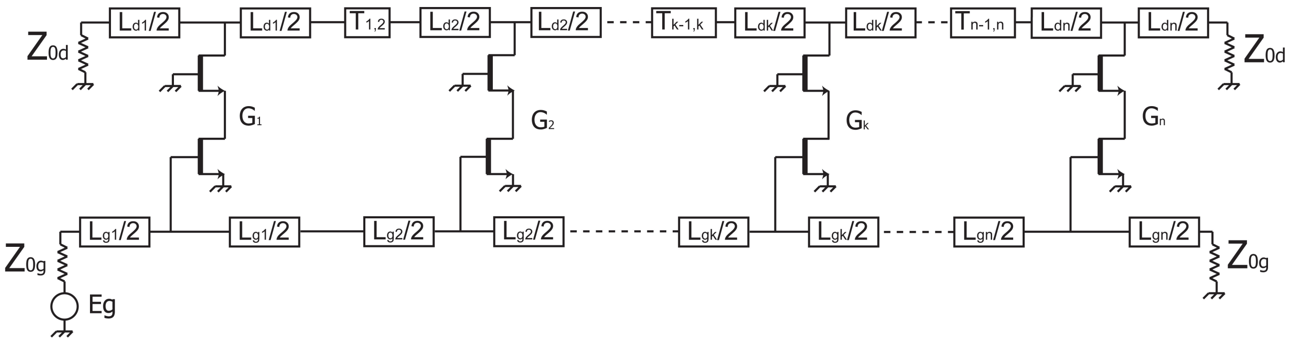

Figure 2: *Block diagram of the MMIC Distributed Transversal Filter (Bias circuit not shown)*

$Z_{0g} = \sqrt{\frac{L_g}{C_{in}}}$. Similarly, $Z_{0d} = \sqrt{\frac{L_d}{C_{out}}}$ is the characteristic impedance of the drain line formed by the inductance L_d and the output capacitance of the cascode. In this implementation both characteristic impedances are set to be equal to 50Ω.

Drain and gate lines together give rise to a time delay per stage approximately given by the following relation

$$t_{LCk} \approx \sqrt{L_{gk}C_{ink}} + \sqrt{L_{dk}C_{outk}} \tag{5}$$

Additional delay has to be inserted between the stages in order to satisfy the encoding and decoding temporal response criteria. These can be implemented using matched (i.e., with characteristic impedance equal to the ATL) microstrip transmission lines taking advantage of the flat group delay provided by such structures. Alternatively, it is possible to build an artificial transmission line by periodically placing additional capacitors in a microstip line with high characteristic impedance. The former option gives rise to less attenuation in the line and flatter group delay while the second provides larger time delays for a given chip area. In this work microstrip transmission lines with $Z_0 = 50\Omega$ were used to implement the additional delay.

4 Simulation Results

All the results were obtained using Advanced Design System ADS2005A$^{\mathrm{TM}}$by Agilent. Figure 3 shows the time response of a 5-stage encoder with delays and gains set to the sequence ”101101010” and a rate of 40 GChip/s.

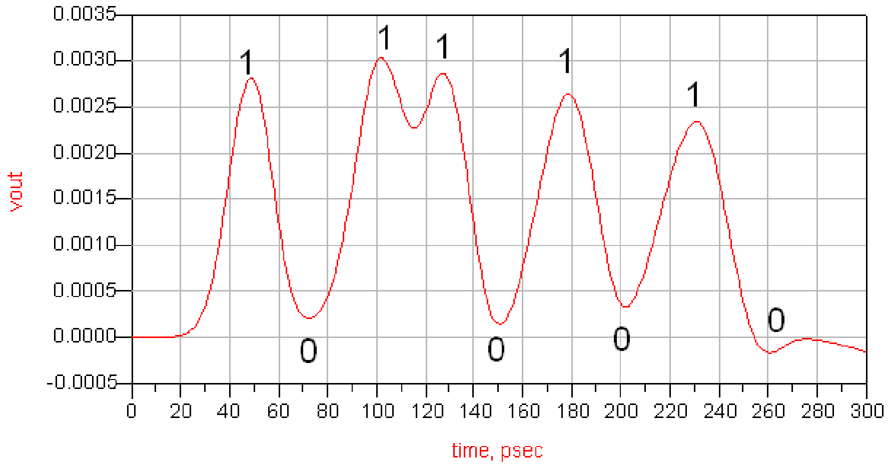

Figure 3: *Transient response of the encoder tuned to the sequence ”101101010”*

In figure 4 we show the gain and reflection parameters of the circuit. One can observe from S11 that the encoder has a good input match up to 30 GHz, which is sufficient for 40 Gbit/s operation.

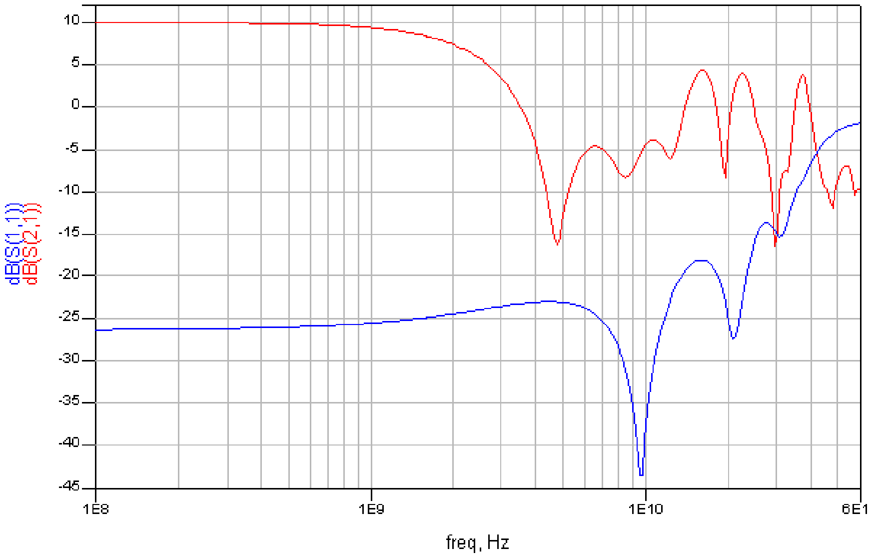

Figure 4: *S11 and S21 of the encoder tuned to the sequence "101101010"*

5 Conclusions

A Distributed Transversal Filter for CDMA encoding and decoding applications has been proposed. The encoder was successfully designed and simulated. This new concept, where the number of stages is equal to the number of "positive" chips of the CDMA codeword, allows the use of longer codewords so number of users in the network is increased. Future work will focus on the design of a DTF with switchable delays, i.e., the time delay between taps is no longer fixed but can be set by software according to the codeword. We are considering the use of Micro Electro Mechanical System (MEMS) for such purpose.

References

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