Verification of FPGA Generated SEFDM Signals [1]

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Abstract

Simulation, using a model of a system or process, is widely accepted as a method of qualification and evaluation of complex systems. The success of a simulation depends on the accuracy of user defined values which model parameters gathered by analytical or empirical methods. In situations where some parameters are unknown or difficult to quantify, it is required to perform the system operations in a real-world situation. Often, moving from a simulation environment to a hardware environment can result in considerable development and implementation challenges. Hence, simulation in conjunction with hardware, so called *in the loop* validation, can provide a fast method for verification and a reduction in development time. This paper concerns the successful signal transmission of a recently proposed communication scheme, termed as Spectrally Efficient Frequency Division Multiplexing (SEFDM). Signal transmission is verified using in the loop methodology. Experimentally generated signals from a bespoke reconfigurable Field Programmable Gate Array (FPGA) are sampled, using an oscilloscope and compared with an analytical model of SEFDM transmitter.

1 Introduction

Implementation of multi-carrier wireless systems in FPGA is commonplace [1] [2]. Work on refinement of multi-carrier modulation methods, such as SEFDM [3], represents one of a number of emerging techniques which enable a reduction of the bandwidth required, without a corresponding penalty in data throughput and with tolerable penalty in error rates [4]. Related techniques include Faster-than-Nyquist (FTN) [5], Overlapping Orthogonal Frequency Division Multiplexing (OvFDM) [6] and High-Compaction Multi-Carrier Modulation (HC-MCM) [7]. It has been shown that, by applying common measurement criteria such as Peak to Average Power Ratio (PAPR) [8], SEFDM has desirable properties for wireless communication. It has also been demonstrated that SEFDM transmitters can be successfully implemented in FPGA hardware [9] and subsequently targeted towards Application-Specific Integrated Circuit (ASIC) [10]. Section 2 details the in the loop verification methodology with a description of the variables used, a summary of the best performing variable settings and numerical quantification of sampling rates at each verification stage. Section 3 provides experimental signal verification results against transmitter models and the work is concluded in Section 4.

2 Verification Methodology

The system reported employs a hybrid hardware, test equipment and software topology. Hardware refers to an FPGA-based wireless signal generator with independent I and Q channels and a maximum output bandwidth of 125MHz per channel [11]. The test equipment employed is a real-time oscilloscope capable of sampling rates from 10MS/s to 20GS/s. The software element is where the oscilloscope-sampled experimental signal from the FPGA hardware is phase aligned with an analytically generated signal to quantify the error between the experimental and analytical signals.

2.1 General description

The transmitter verification process is shown diagrammatically in Fig. 1. Conceptually, the methodology is divided into four interconnected blocks, cross-referenced to the Figure in bold text. The **FPGA hardware** serves as the transmitter which generates analogue signals from numerically defined source data. This is followed by the **Real Channel** which is a physical connection (cable or wireless) from the Digital to Analogue Converter (DAC) in the FPGA block, to the input of the **Oscilloscope**. The oscilloscope is a sampling scope which outputs a sampled representation of its input analogue signal at rates and filtering set by the user. The **Matlab TX Model** comprises a set of mathematical functions which model the transmission process (both analytically and architecturally). These models are used for comparison to the sampled data fed to the **Matlab TX Model** as an ASCII file from the **Oscilloscope**.

2.2 Methodology description

Complex source data (I_IN, Q_IN) of size N serves as the input to an FPGA based SEFDM transmitter. The FPGA presents to the DAC N time samples at data rate F_D. If F_D is lower than the DAC source clock F_DACCLK, the resulting analogue signal is constructed from N_S samples which is greater than N; otherwise N=N_S. This signal is transmitted over a channel and then sampled by the oscilloscope, at rate F_SCOPECLK, producing N_O samples (where N_O > N_S). This data can either be passed directly to the TX Model, or first be subjected to filtering at frequency F_SCOPEF. The same complex data applied to the FPGA hardware serves as source data for two models; namely an analytical model of the complex SEFDM generation process and a model of the FPGA architecture. The aforementioned N_O sample points and the resulting model(s) output

[1] This paper is based in part on a recent submission to Reconfig'2011 with the title: "A Verification Methodology for the Detection of Spectrally Efficient FDM Signals Generated using Reconfigurable Hardware".

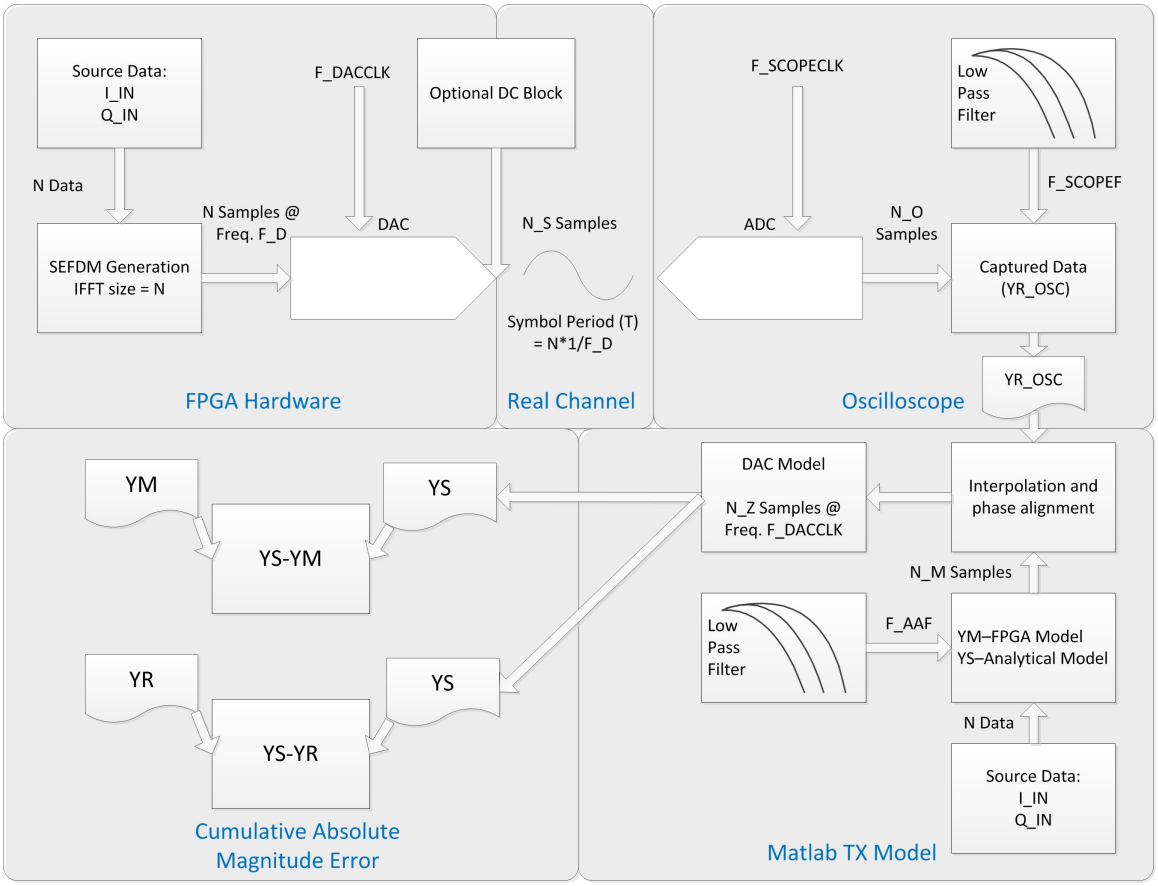

Figure 1: Verification methodology block diagram

data points (N_M) are made equal using interpolation. This is performed so that an accurate comparison can be made between the experimental and model signals and furthermore so that the experimental signal can be phase aligned to the analytical model. The sampling rate used to capture the experimental signal sets an upper bound on the phase adjustment/timing adjustment that can be made, defined in Eq. 1:

$$MaximumPhaseAlignment = \frac{1}{F\_SCOPECLK} \tag{1}$$

As the output of the transmitter has no phase reference, setting F_SCOPECLK = F_DACCLK (this meets Nyquist as F_BW = F_DACCLK/2) would provide a 4nS phase adjustment step. Ideally, the phase alignment step size is required to be as small as possible, but in reality is constrained by current available devices. Hence, F_SCOPECLK is set as F_DACCLK*4 which results in a phase adjustment of 1ns and a corresponding 1GHz sampling clock.

2.3 Input data and settings

It is not possible to evaluate large sequences of source data, due to the verification time required for each sequence. Therefore, in order to serve as source data for the purposes of confirming the correct operation, a set of real-only source data sequences is selected at random from 256 possible sequences and is defined in Table 1. Furthermore, based on empirical data, the variable settings which represent the highest performing, in terms of experimental against analytical signal error is provided in Table 2.

2.4 Sampling rate discussion

The previously detailed DAC clock value, F_DACCLK, is fixed at 250MHz. Thus, every 4ns and on the rising edge of F_DACCLK, the digital input value presented to the DAC is translated to a proportional output voltage. The resulting analogue output signal has an effective maximum communications bandwidth, F_BW defined in Eq. 2 as:

$$F\_BW = \frac{F\_DACCLK}{2} \tag{2}$$

Hence, the spectral properties of the data presented to the DAC cannot exceed F_BW without suffering aliasing effects. The resulting SEFDM symbol period (T) can also be defined, based on N and F_DACCLK, as shown

Table 1: Input data sequence selected for transmitter verification

Seq. ID	Data Value							
1	+1	-1	+1	-1	+1	-1	+1	-1
2	+1	+1	-1	-1	+1	+1	-1	-1
3	+1	+1	+1	+1	-1	-1	-1	-1
4	+1	+1	+1	+1	+1	+1	+1	+1
5	-1	-1	-1	-1	-1	-1	-1	-1
6	+1	+1	+1	-1	-1	+1	+1	+1
7	+1	-1	-1	-1	+1	+1	-1	-1
8	+1	-1	-1	+1	+1	+1	-1	-1
9	+1	-1	+1	-1	+1	-1	+1	-1
10	-1	+1	-1	+1	-1	+1	-1	+1

Table 2: Best performing value settings used for transmitter verification

Variable	Value	Unit
F_D	250	MHz
F_BW	125	MHz
F_DACCLK	250	MHz
F_SCOPECLK	1000	MHz
F_AAF	Off	N/A
F_SCOPEF	Off	N/A
N	32	Points
N_O	256	Points
N_M	32	Points

in Eq. 3. Due to the architecture utilised for the transmitter, N is both the number of time samples and the inverse transform size,

$$T = \frac{1}{F\_DACCLK} * N \tag{3}$$

As F_D is set to be equal to F_DACCLK, the number of points which represents an SEFDM symbol in period T is N and hence, N_S=N. When sampling is applied by the oscilloscope, the resulting samples N_O can be defined in Eq. 4 as:

$$N\_O = \frac{F\_SCOPECLK}{F\_DACCLK} * N\_S \tag{4}$$

Over the same period T, the oscilloscope will collect 256 samples (at 1GHz) of a analogue signal created using 32 samples (at 250MHz). hence, the oversampling factor is 4 as a ratio of F_SCOPECLK and F_DACCLK. Interpolation between this experimental signal, the analytical and the architectural models (which consists of N_M points) is required to enable a comparative analysis.

3 Results

Recalling from Section 2, the experimental time signal is compared to an analytical model and an FPGA architectural model for the purpose of cumulative absolute magnitude error quantification. This error δ is defined in Eq. 5

$$\delta = \frac{\|S_{ref} - S'_{comp}\|}{\|S_{ref}\|} \tag{5}$$

where S_{ref} is the reference analytical model time-domain signal, while S'_{comp} is either the experimental signal or the FPGA architectural model signal, each of which is scaled appropriately. The cumulative absolute magnitude error which equates to an average for each sequence (defined in Table 1) over 32 time samples is found in Fig. 2. For the architectural model, three plots are provided each with a different scaling factor based on a logical right shift operation (bit scaling). Furthermore, Fig. 2 also provides the result of a study into the best performing bit scaling when applied to various input amplitude values and operational values defined as *scale amplitude*). The results in Fig. 2 show that for the same input signal and the same bit scaling factor, the experimental and architectural signals have similar error trends and very close error values. The small difference in error values is attributed to the fact that the experimental system not only uses real electronic components but also a real transmission channel. Conclusively, the procedure used to generate the experimental signal is deemed correct. It can also be seen that a reduction in scaling applied (for example from 8-bit to 6-bit) results in a corresponding reduction in error. The result also provides evidence of the optimum configuration of input amplitude and scale

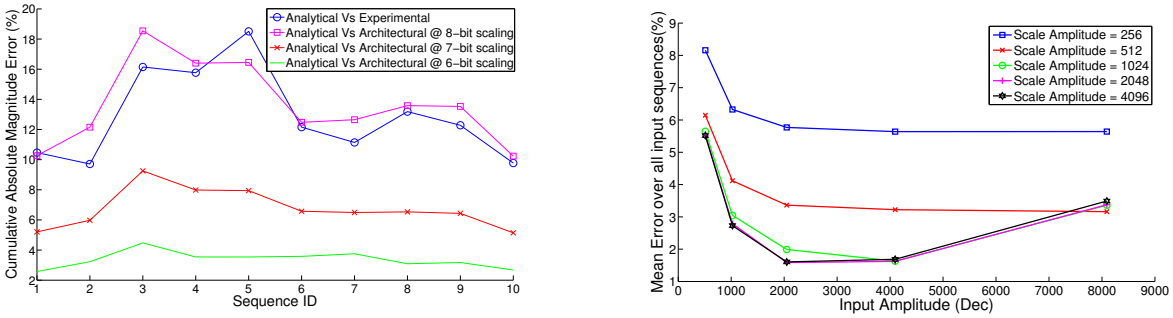

Figure 2: Cumulative absolute magnitude error for experimental and architectural signals with different bit scaling against analytical signals (left) and error performance with different internal and external data amplitudes (right)

amplitude values against the aforementioned bit scaling operation applied. The optimum setting is found to be 2048 for both amplitude values with a 6-bit scaling factor applied. The mean error, using the optimum values, between the analytical signal and architectural signal (and therefore the experimental signal) is 1.5 %. Future investigation will confirm the result by use of the optimum settings in the real hardware for comparison with the simulated result.

4 Conclusion

This work reports a verification methodology which demonstrates the success of generating real SEFDM signals using reconfigurable hardware and hence, that SEFDM is adaptable for use in hardware. Verification is provided of the experimental signals, whereby an architectural model and the experimental signals have similar error when compared to an analytical model and thus serve as confirmation of the correct experimental signal properties. Further analysis of the transmitter hardware architecture is provided such that an optimum configuration, within the current hardware limitations, of data input and internal amplitude values is derived to produce a minimum error between simulation and hardware signals.

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