Digital femtosecond time difference circuit for CERN's timing system.

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Abstract: This paper presents a novel digital circuit, based on the analog Dual Mixer Time Difference circuit, developed by David W. Allan, designed to characterise oscillators frequency stability. The proposed digital circuit, named Digital Dual Mixer Time Difference (DDMTD), is capable of measuring time differences between two digital clock signals with very fine resolution (subpicosecond) using a relative low frequency counter.

1 Introduction.

Timing systems are specialised networks that provide a common notion of time in a distributed environment. In other words, they ensure that all clocks in the system are ticking at the same speed and showing identical time at every instant.

Accurate time synchronisation is a major requirement in many real-time applications. Distributed control systems, factory automation and data acquisition systems all require the execution of operations with very tight time constraints. This becomes particularly difficult in large-scale systems, such as CERN's accelerator complex, where distances between nodes are in the range of tens kilometres, causing long and often unpredictable transmission delays.

A proposal for the new CERN's accelerators timing systems aims to increase the timing system accuracy, below 1 ns, as well as multiplexing both timing and control data over a single fibber link by using an Ethernet optical transmission link. The new timing network is foreseen to be deployed on the next sLHC upgrade and will be used for the coming years; a life expectation of this system will be around the 10 years [4]. To maintain a long life of the hardware, at a relative low cost, it would be preferable to bring to the project standardized solutions. This is one of the many reasons why Ethernet was selected to be the link layer for this new timing system. Another standardized technology, Synchronous Ethernet (Sync-E) proposed by ITU [7] in 2008 is used as a mean to distribute frequency between Ethernet nodes.

The IEEE 1588, also know as Precise Time Protocol (PTP), is as IEEE standard that synchronizes timing nodes using the network layer [5]. PTP is currently being used by several industries to delivery precise timing; the reported best accuracy is on the hundred of microseconds [6].

By combining Sync-E and IEEE 1588 a better timing accuracy distribution between nodes is achieved without the cost of increasing network bandwidth. However in the case gigabit Ethernet (GbE) standard where the recovery clock frequency is of 125 MHz, the accuracy of the timing network is limited to 8ns. To achieve the required timing performance of sub nanosecond it is necessary to design a circuit that is able to measure time differences below the picoseconds range [2]. In addition to that, the links length is foreseen to be long, around 10 km, generating delay variations, due to temperature changes, in the timing network. For this reason there is the need to measured and compensated these variations on the flight without the cost of increasing the network bandwidth.

This paper presents a novel circuit, the Digital Dual Mixer Time Difference (DDMTD), which acts as digital phase detector capable of femtosecond time resolution using a relative low frequency counter and it is organized as following. Section 2 introduces the DDMTD circuit followed by the theoretical analysis of its performance. The intrinsic problem of this circuit, glitches on the output clock, is explained and it's followed by the description of techniques used to remove them. Section 3 presents a simulation of the DDMTD using the difference deglitching techniques where the performance of the DDMTD is here perceived. While section 4 concludes this paper.

2. Digital Dual Mixer Time Difference

The Dual Mixer Time Difference (DMTD), first presented by David W. Allan, consists on comparing two clock signals in order to know the frequency and phase deviation from the reference oscillator [1].

The DMTD is an analog technique that can measure time differences with high precision using a commercial time interval counter [1]. However limitations arise when the application [2] requires the continuous evaluation of phase difference between two digital timing signals.

In order to have a digital circuit capable of measuring time differences of digital signals with a fine time resolution a digital version of the DMTD has developed. This circuit, named as Digital Dual Mixer Time differences (DDMTD), has two D Flip-Flops, plus a deglitching circuit that removes unwanted glitches and a time difference frequency counter. The DDMTD circuit schematic is shown in figure 2.

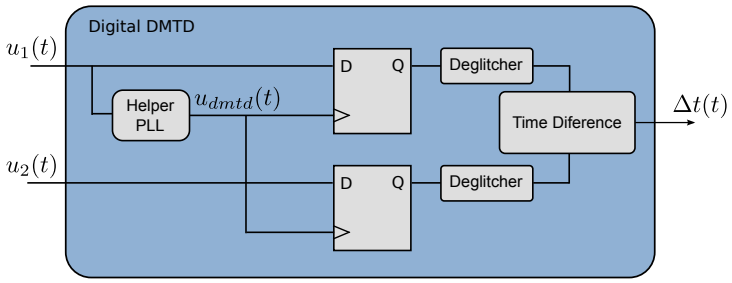

Figure 1 - Digital DMTD

The differences between the analogue DMTD design and the one just presented are easy to enumerate: the input clock signals $u_1(t)$ and $u_2(t)$ are squared waves with fundamental frequency v_n and a phase of $\theta_a(t)$ and $\theta_b(t)$ respectively: The analog mixers are substituted by D flip-flops: It doesn't require a low-pass filter after the mixers, however for very fine time resolution, below the picosecond, a deglitch circuit is necessary. The glitches occur due the presence of phase noise in the timing signals and as well due to the possible metastability phenomena which is caused by the small sweep in frequency that might violate the setup and hold time requirements of the flip-flops [3].

The Helper PLL, shown is figure 1, has the task of generating the $u_{dmtd}(t)$ signal whose fundamental frequency, v_{dmtd}, can be defined has:

$$v_{dmtd} = \frac{N}{N+1} v_n \tag{1}$$

Where N is an integer number. Easily to verify is that the higher N is, the small is the difference between the frequency signals v_{dmtd} and v_n, this frequency difference is represented by v_{beat}.

A time diagram of the DDMTD flip-flop's outputs, for an N=5, is presented in figure 2.

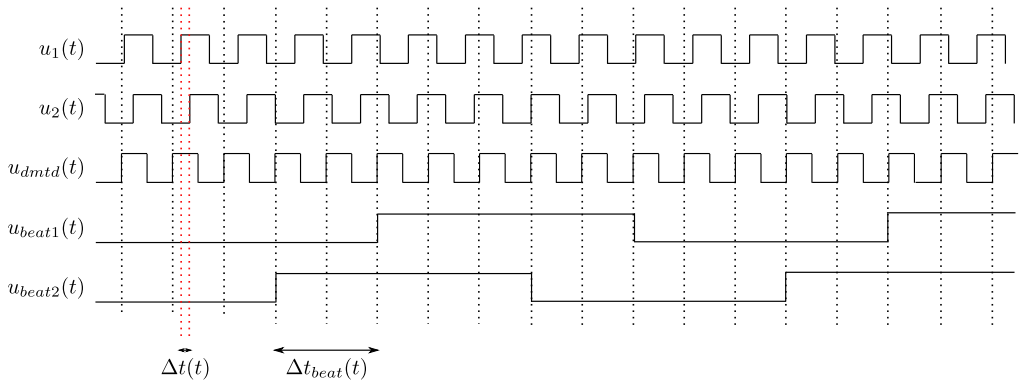

Figure 2 - DDMTD output for a N = 5

Due to the edge sampling of the flip-flops the minimal time resolution is bounded by:

$$\Delta t_{\min} = \frac{1}{v_{dmtd}} \frac{v_{beat}}{v_n} = \frac{v_n - v_{dmtd}}{v_{dmtd} v_n} = \frac{1}{N v_n} \tag{2}$$

Equation (2) shows that the minimal time resolution decreases as N increases. In order words, the close is the frequency v_{dmtd} to v_n the smaller is the DDMTD time resolution. The DDMTD can reach very fine time resolution as shown by (2), for N=8192 (v_{beat} = 15.26 kHz and v_n = 125MHz) the time resolution is 946 fs.

The time difference, $\Delta t(t)$, between $u_1(t)$ and $u_2(t)$ is given by,

$$\Delta t(t) = \Delta t_{beat}(t) \frac{v_{beat}}{v_n} \tag{3}$$

Where $\Delta t_{beat}(t)$ is the time difference between the positive transitions of both $u_{beat1}(t)$ and $u_{beat2}(t)$, as depicted in figure 2.

However the output of the flip-flops starts to show glitches as the time resolution increases. This occurs due to the fact that the DDMTD starts to sample the jitter from timing signal. Figure 3 shows the output clock from the flip-flops where we can see the occurrence of the glitches described. The jitter of the timing signal, being a random process, makes the DDMTD to sample in some occasions a "1" value and in others occasion the "0" value. Figure 4 shows an edge transition snapshot measured from the flip-flop output, the random nature of the jitter is in this figure well represented.

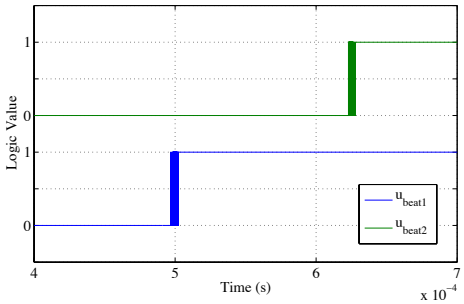

Figure 3 - Glitch on the output clocks

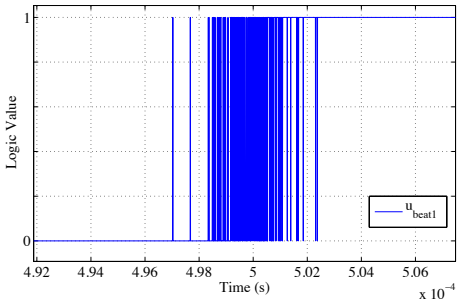

Figure 4 – Glitch on the output clock

These glitches need be filtered and removed and this can be achieved by adding a digital deglitch circuit that, according to its deglitching algorithm, removes the glitches and thus preventing erroneous measurements.

Several deglitching techniques are described:

- First Edge – selects the first positive edge as a good edge for the time differences counter.
- Mean Edge – selects the as the best edge the mean edge between all the glitches.
- Zero Count – counts the numbers of "1" and "0" and selects as the best edge the time position where the number of zeros is the same as the number of ones.

The deglitching techniques need to be very simple due to the fact that they are going implemented in hardware where the resources are limited.

3. Simulations

Simulations were conducted to verify the performance of the DDMTD as digital phase detector with the deglitching techniques proposed. The input timing signals $u_1(t)$ and $u_2(t)$ have 10 ps of rms jitter and the time difference between both timing signals is of 1ns.

Table 1 – Time Difference Error Measurement using a 125 MHz frequency counter

	Error				
	$v_{beat}(Hz)$				
Algorithm	**10M**	**1M**	**100k**	**10k**	**1k**
First Edge	670ps	67ps	5ps	581fs	79fs
Mean Edge	670ps	67ps	5ps	560fs	26fs
Zero Count	670ps	67ps	5ps	521fs	10fs

Table 1 shows the time difference error measured by the DDMTD circuit. Easy to observe that as the v_{beat} frequency decreases the time difference has better accuracy. The difference deglitching techniques have difference performance that starts to be more obvious as the time resolution increases. The algorithm that has the best performance is the Zero Count algorithm. At a 1 kHz the Zero Count algorithm shows a time difference error that is two times better than the Mean Edge and is eight times better than the First Edge. These results show that the deglitching techniques employed influence the time difference measured by the DDMTD circuit.

5. Conclusions

In this paper it has presented a digital architecture for the dual mixer time difference, its has several advantages over other phase frequency detectors like having a linear scale over its full range; The measurement can be done directly from a relative low frequency counter without adding any analog components. The circuit phase accuracy its limited by the v_{beat}. The timing signal phase noise generates glitches in the output of the flip-flops when the time resolution is increased. They are filtered and removed by adding to the flip-flop output's a deglitching algorithm. The "zero count" algorithm has the best performance in filtering and removing the glitches. The measurement presented has a fine time resolution with a linear characteristic, which makes it an attractive solution to measure dynamics delays in the transmission link in order to set the latency bounded.

References.

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