Light induced instability in bilayer nc-Si/a-Si thin film transistors

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Abstract: Bi-layer nanocrystalline silicon TFTs were investigated and their stability evaluated under broad range of stress conditions. While bi-layer TFTs exhibit high electrical stability in the dark, it largely deteriorates when TFTs are stressed under illumination. However these TFTs do not exhibit persistent photoconductivity, unlike some other large area orientated material systems. Amorphous silicon cap layer is shown to be unable to provide sufficient protection from light through absorption.

1 Introduction.

Amorphous silicon thin film transistors are widely used in a range of large area applications such as displays and detectors [1, 2]. Nanocrystalline silicon (nc-Si:H) have been used as the channel layer in thin film transistors (TFTs) and photovoltaic solar cells [3]. It benefits from higher stability, higher mobility, and suitability for large area, low cost fabrication on plastic compatible substrate temperatures [4]. However due to its higher dark conductivity is suffers from the high off current and low ON/OFF ratio. This issue has often been suppressed by capping the nc-Si:H channel with a layer of a-Si:H. Although this approach leads to some reduction in the field effect mobility of the device due to the higher contact resistance, it increases the ON/OFF ratio to a level acceptable for the device applications [5].

In many areas of TFT applications, devices are subjected to direct (e.g. phototransistors) or indirect (e.g. AMOLED displays) illumination. Therefore it is important to investigate the effect of TFT stability when subjected to illumination and/or electrical stressing. In this work we investigate the stability of a-Si:H/nc-Si:H TFTs stressed under bias, illumination and combined bias-illumination and compare it with the previously reported results of dark bias and light stress [6]. We also briefly discuss the possible causes of instability in each case.

2. Experimental setup.

The schematic of measurement setup is given in the Fig. 1. The device instability was investigated by measuring the transfer characteristics of the device during stress and recovery. Threshold voltage shift and sub-threshold slope was extracted from it. The durations of stress and recovery periods were 3 hours and 9 hours respectively. Stress conditions are given in the Table 1. Stress was interrupted every 20 minutes and transfer characteristics were measured in the dark in order to be able to compare extracted instability. All recovery experiments were performed with grounded drain and source electrodes. The typical duration of I-V sweep was 30 seconds. All measurements were performed inside a shielded probe station, using Keithley 42000-SCS. Broad spectrum halogen lamp was used for the light stress experiments (Fig.1 inset). The illumination intensity on the sample surface was 60mW/cm^2.

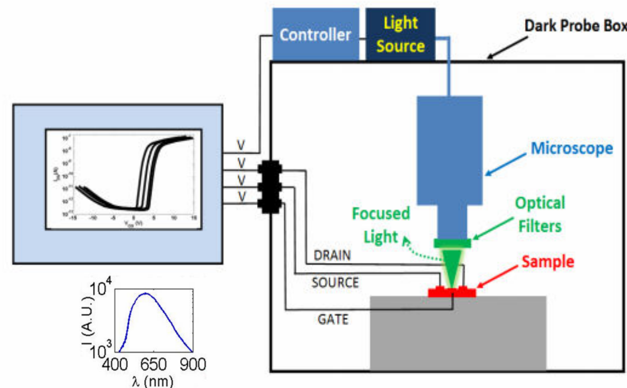

Figure 1. Experimental setup of for measuring TFTs. Spectrum of the illumination source is given in bottom left

All channel layer and insulator films were deposited using RF PECVD. Nanocrystalline silicon was deposited using highly hydrogen diluted silane at a ratio of 100 (H_2/SiH_4=200/2 sccm) at 280°. The pressure of the deposition chamber was set to 900 mTorr and RF power was 10 mW/cm^2. It is very important to have small incubation layer for the bottom gate TFTs due to the accumulation taking place near the bottom channel/insulator interface. TEM experiments show that nc-Si film has very low incubation layer and high crystallinity. Crystallite columns start forming close to the channel. The thickness of the nc-Si active layer is 15 nm and it was capped with 35 nm a-Si layer.

The bottom gate inverted-staggered TFT was used in this work. After a three step solvent cleaning and oxygen plasma etching of any organic contamination layer, the substrate was loaded in a thermal evaporator to evaporate a 50nm layer of Cr for the gate electrode. This layer was patterned using standard Cr etchant and loaded in the PECVD for the deposition of the tri-layer. The tri-layer consisted of an active channel layer (a-Si:H/nc-Si:H) sandwiched between two SiN:H (300nm gate and 150nm passivation) layers. The first SiN:H would serve as the gate dielectric and the second as a passivation nitride and etch stop. The top SiN:H was patterned and etched using buffered HF to open contact areas before the PECVD deposition of the bi-layer. The bi-layer consists of a n+ nc-Si:H contact layer and a SiN:H (150nm) passivation nitride and was patterned using buffered HF (to etch the SiN:H) and KOH etch to etch the contact and channel layers. A fast HF dip was performed before loading the sample in the PECVD for the deposition of a 150nm SiN:H layer. The single SiN:H layer was patterned and etched using buffered HF. The contact metal layers consist of 200-300 nm evaporated aluminium. It was patterned and etched using wet aluminium etchant.

Results

TFT's transfer characteristics measured under the illumination with different wavelengths are shown in the Fig. 2. The values of light power falling on a-Si layer and on nc-Si layer are given in the legend for each wavelength. The light reaching the a-Si is unattenuated lamp light; however due to the absorption in amorphous silicon cap layer the light intensity reaching nc-Si is weaker. Approximate values were estimated from the spectral absorption coefficient of the a-Si film. It can be seen that even for short wavelengths the nc-Si:H film is exposed to substantial fraction of light. As expected the illumination leads to an increase in the off current of the device, mostly due to the photoconductivity of amorphous silicon, however it does not significantly effects its behaviour in the above-saturation region. This suggests that the density of the photogenerated carriers is significantly smaller that the density of the bias accumulated carriers.

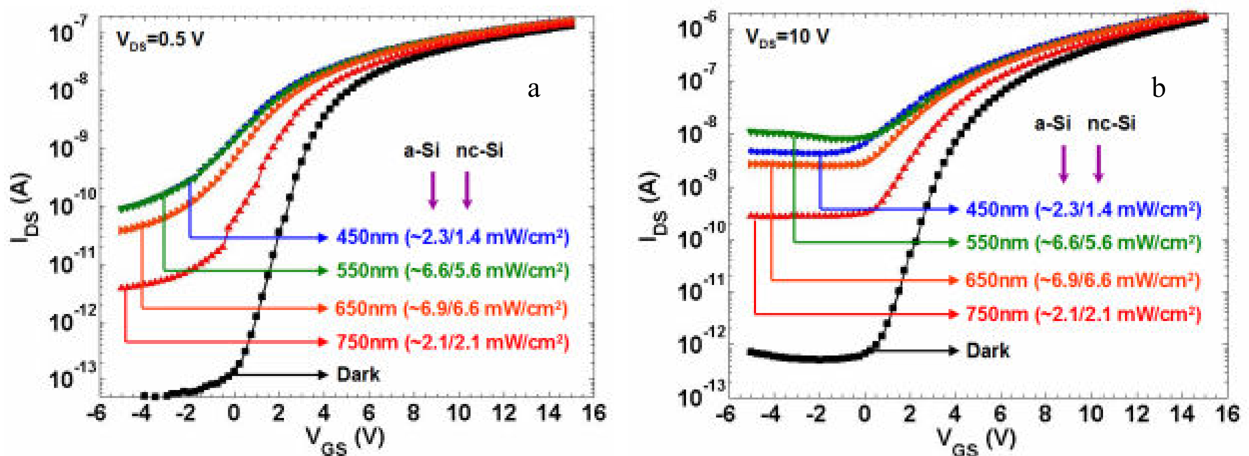

Figure 2. Transfer characteristics measured under different intensities of light at two different drain voltages (a-0.5V, b-10V). Intensities of light falling on the a-Si and nc-Si surface are given in the legend.

To investigate the dynamic of instability, changes in the threshold voltage and sub-threshold slope were extracted from transfer curves which were recorded every 20 minutes (Fig.3a and 3b). It could be noticed that while instability was relatively small under PBS, LS, NBS and NBLS, it strongly increased under PBLS. While V_T shift after NBLS was relatively small, it was still much larger than NBS. Smaller V_T shift under negative bias stress could be explained by the n-type of TFT, where it is much easier to accumulate electron as compared to holes. Same current range was selected for the extractions due to the non-linearity of I_{DS}.

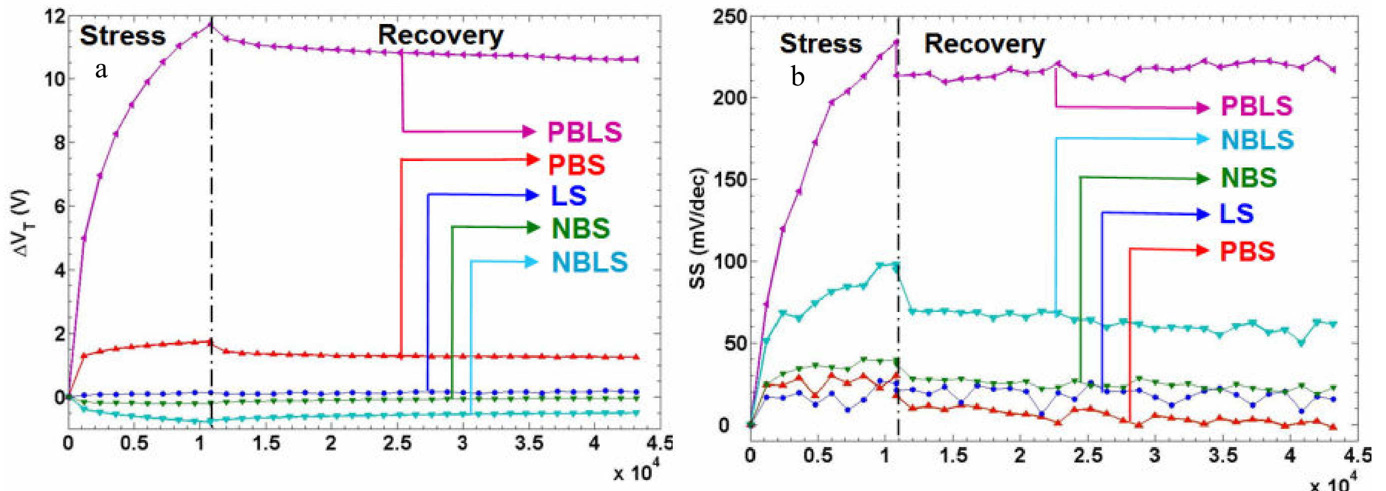

Figure 3. Dynamics of ΔVt and ΔSS under various stress conditions and during recovery.

The stress was followed by the natural recovery in all measurements. It is clear that sub-threshold slope is degrading under combined light and bias stress (both positive and negative bias). These results are consistent with the reported results for nc-Si only devices [6]. This similarity could be be explained by the a-Si cap inability to efficiently screen the nc-Si channel layer from illumination.

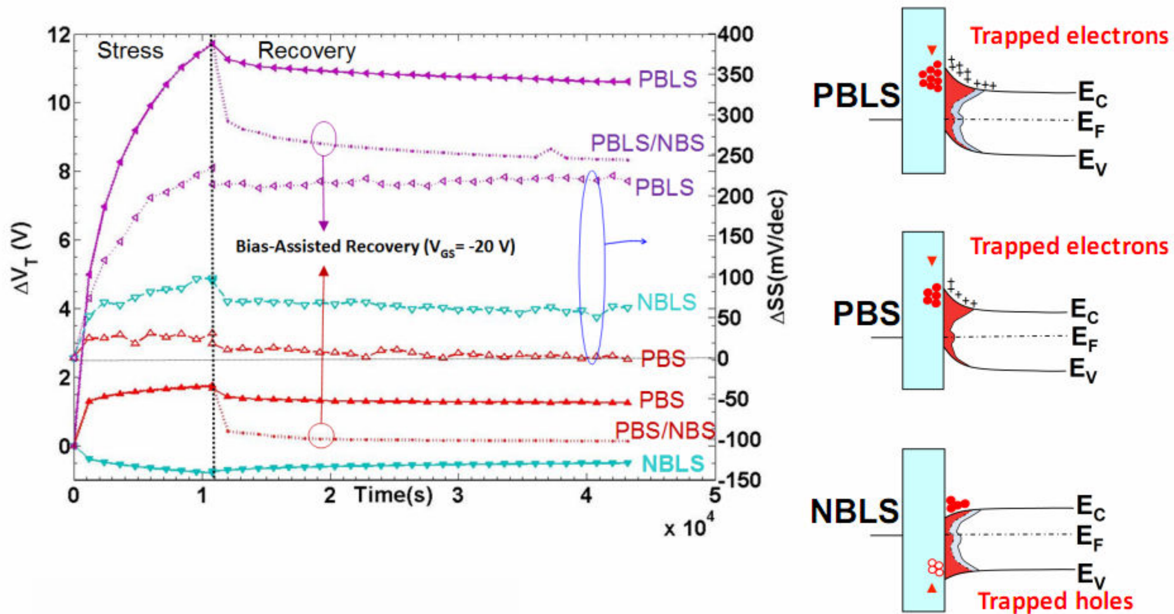

Figure 4. Recovery of ΔVt and ΔSS under natural and forced recovery conditions.

Fig 4 shows V_T shift under stress and during the forced recovery. Initially bi-layer TFTs were stressed under PBS or PBLS and then allowed to recover naturally (no light and no bias). Then the experiments were repeated, however forced recovery was used instead of natural recovery. During the forced recovery Vg=-20V (same conditions were used during NBS) were applied and the devices were kept in the dark. Forced recovery is speeding up the charge detrapping from gate dielectric. It is clear that for both PBS and PBLS forced recovery increased the rate of recovery however the major difference was the recovered fraction of the Vt shift. For PBS almost all of the instability was removed while for PBLS only small part of the VT was recovered. This could be explained by the different instability mechanism – only charge trapping is causing instability under PBS whereas defect state creation becomes the dominant cause for instability under PBLS. The change in the deep defect density in the nc-Si channel and change in the trapped gate dielectric charge are shown on the sketches of the band diagrams (insets of Fig.4) for each case.

6. Conclusions.

Bi-layer nanocrystalline silicon TFTs were investigated and their stability evaluated under broad range of stress conditions. While bi-layer TFTs have a–Si like on/off ratio, electrical stability in the dark is several times better than amorphous silicon TFTs. This stability is associated with the lack of the defect state creation in nc-Si film. However TFTs operating under prolonged illumination still exhibit large increase in instability.

We associate this phenomenon with the defect state creation in the channel due to the recombination of light induced carriers. This is a problem for the devices as instability caused by the defect state creation is more long-lived than that of charge trapping in gate dielectric. Additional shielding is necessary for bottom gate nc-Si TFTs. Alternatively the thickness of a-Si layer could be increased to block more incoming light but compromise should be reached between stability under illumination and the mobility/on-current of the TFT.

Light stress alone is not creating any instability. This is large advantage of nc-Si TFTs comparing them to the other competing material structures, such as metal oxides, where high sensitivity to light is important issue.

Acknowledgments.

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